Educator Hub

Intro to Memory Packaging

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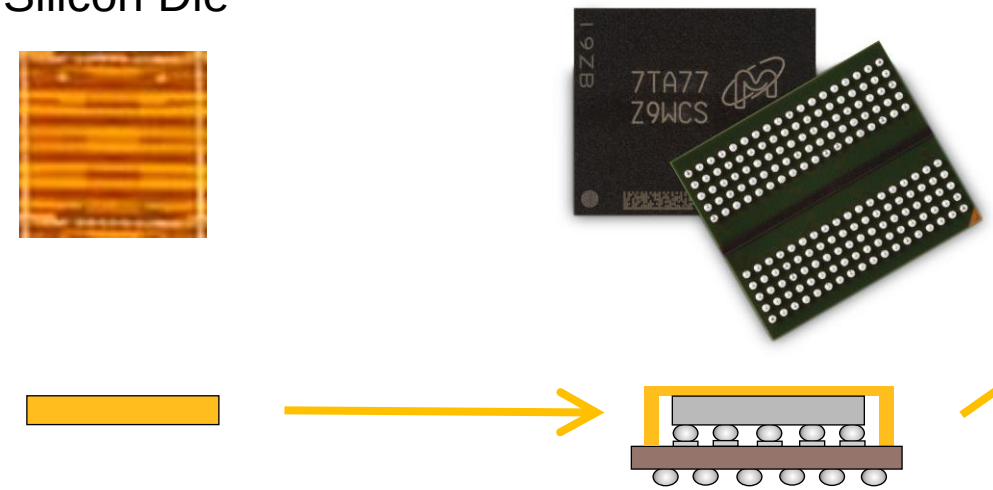
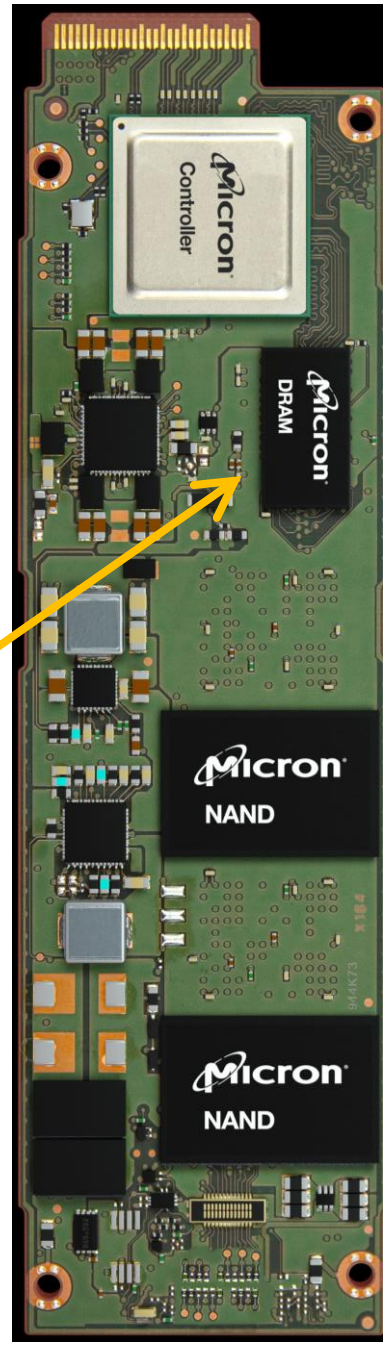
Introduction to Packaging

The semiconductor package is the components surrounding a memory die that enables its use in circuitry.

Silicon Die

Package



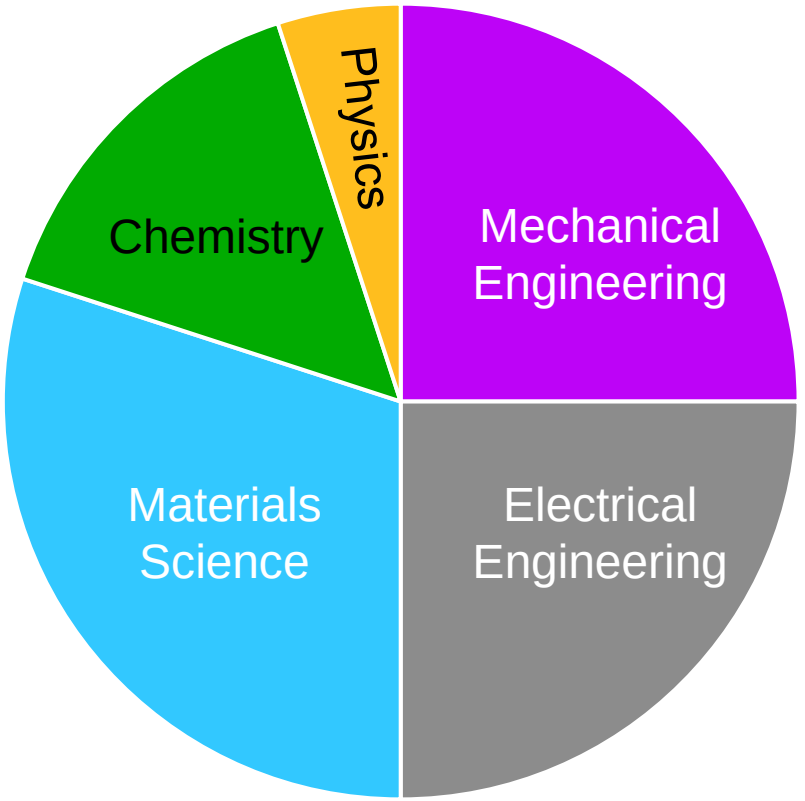


Circuit Board

What goes into making Semiconductor Packages?

Silicon integrated circuits

Metal plated contacts

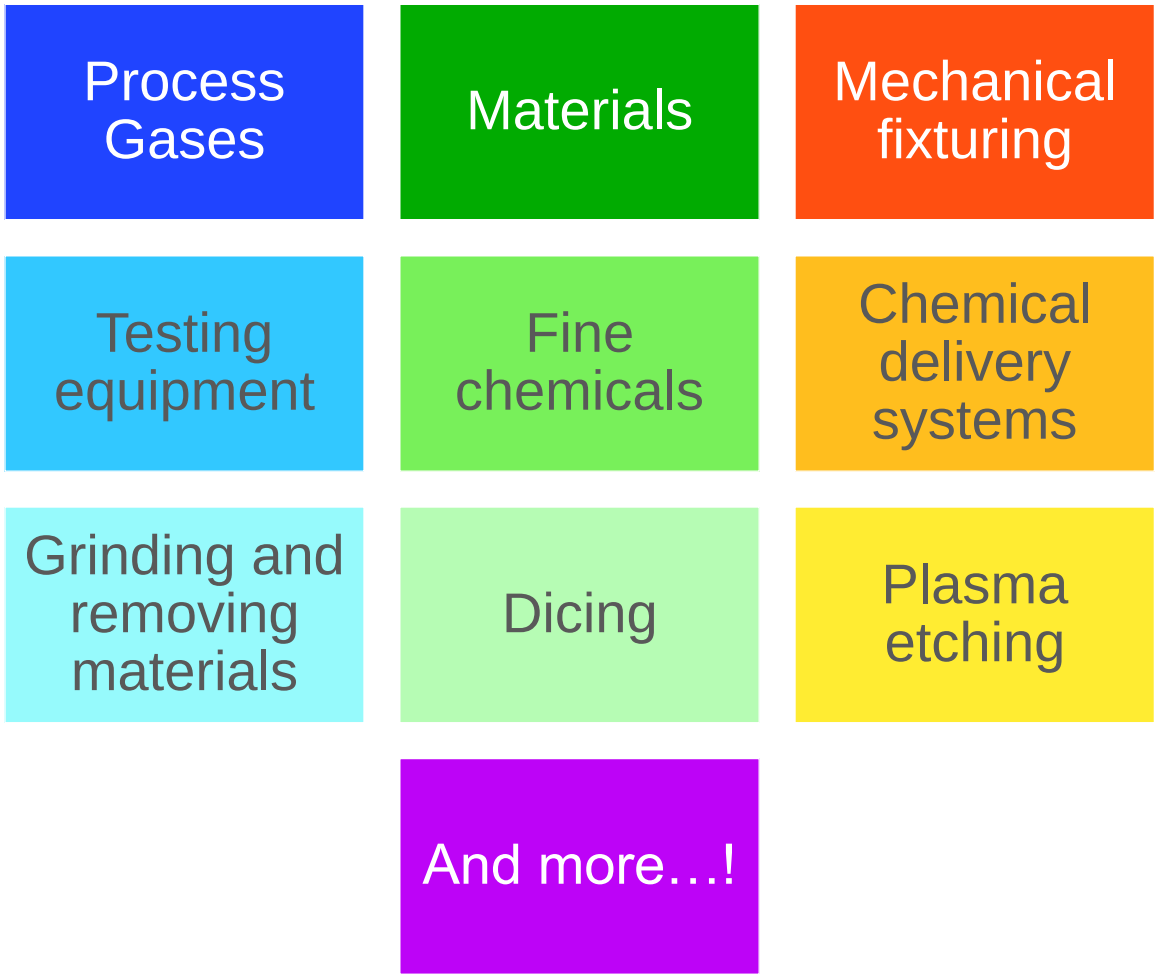


Underfill mold compounds and epoxies

Bonding physics and chemistry

Solder bumps

Additional Tasks



Very diverse ecosystem and knowledge base to develop and deploy semiconductor packaging!

Introduction to Packaging

A) Silicon Die
- Semiconductor Memory

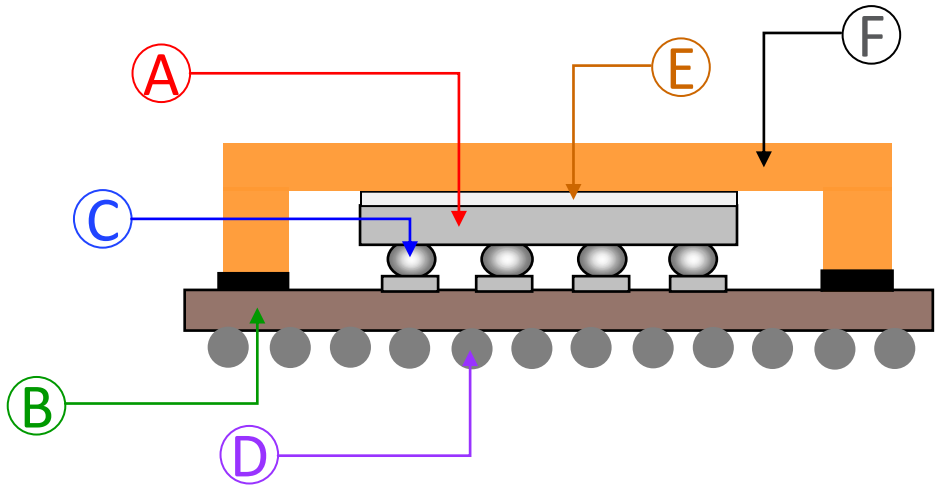
B) Interposer
- Die support
- Embedded interconnects

C) Secondary (die-to-package) Interconnects
- Wirebonds, bumps, or pillars

D) Primary (package-to-board) Interconnects
- Leads or solder balls

E) Heat Dissipation
- Heat sinks/spreaders
- Thermal Interface Materials

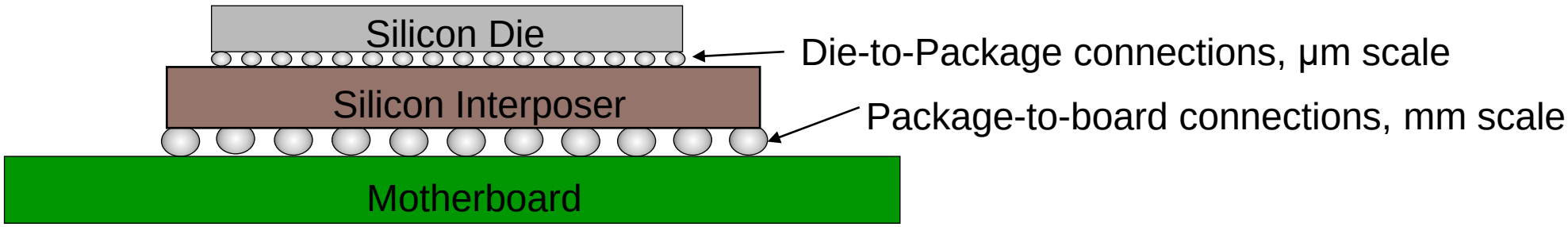
F) Environmental Protection
- Plastic/ epoxy seal
- Ceramic/ metal lid



Introduction to Packaging

What purpose does the package serve?

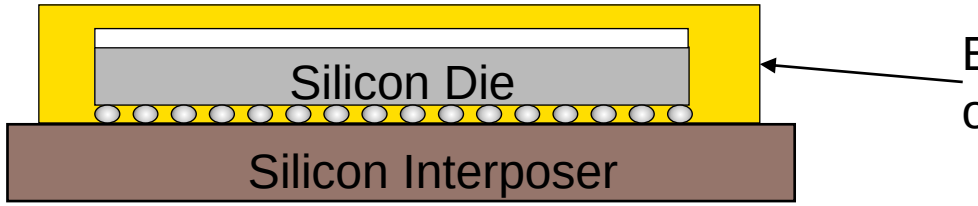
1. Electrical interface between the chip and outer circuitry:
    - Can “adapt” between the different scale size of metal connections on the die to wires on circuit.
    - Improves the quality of signal transmission.



Introduction to Packaging

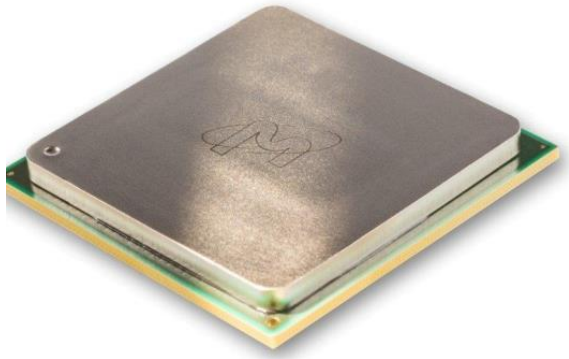
What purpose does the package serve?

2. Physical protection of die:
   - Thinly diced silicon die are fragile and susceptible to mechanical stresses and environmental contamination.



Plastic Encapsulation: Injection molding process encases the assembled die in rigid plastic.

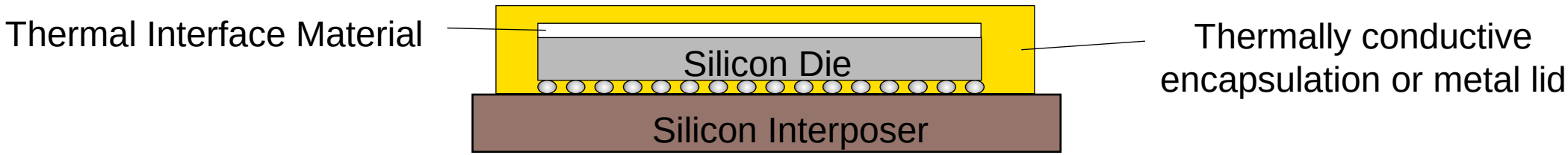
Metal Lid: Assembled die is sealed under a metal lid.



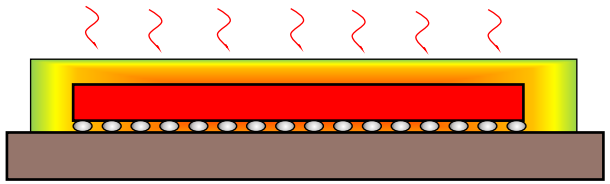
Introduction to Packaging

What purpose does the package serve?

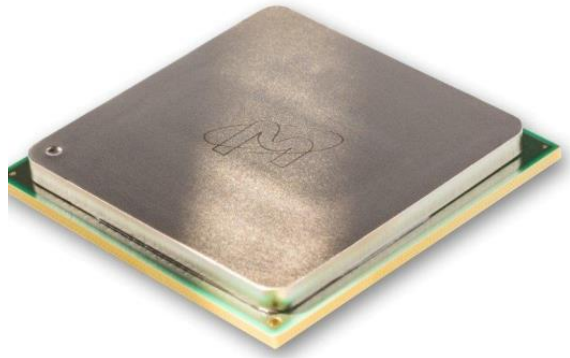
3. Heat dissipation:
   - Complex integrated circuits produce a lot of heat that can burn up a die without the heat dissipation of the package.



Thermally Conductive Fillers: Thermally conductive encapsulation materials can help conduct heat away from the die.



Heat Spreader: Metal lids can also effectively spread heat across a greater surface area.

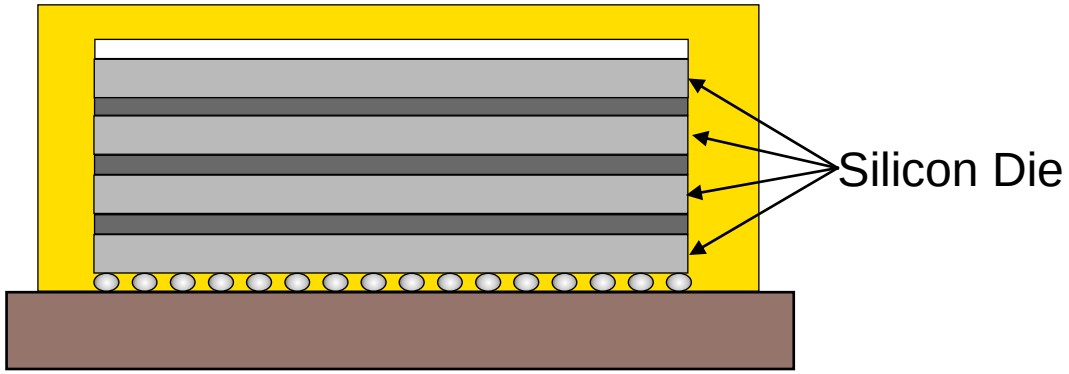


Introduction to Packaging

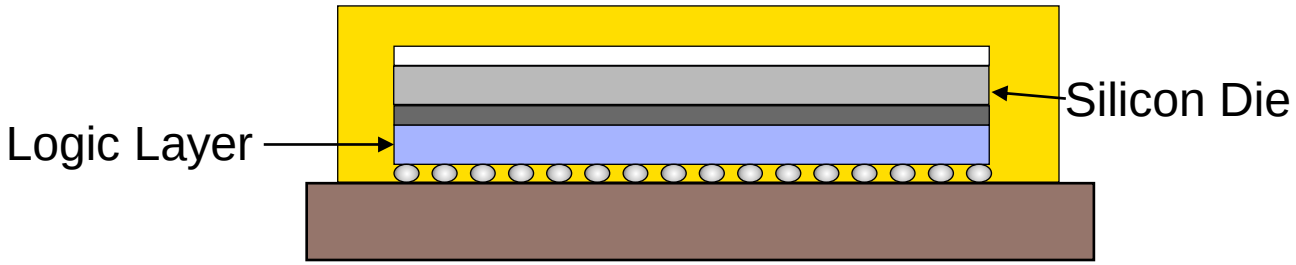
What purpose does the package serve?

4. Expand functionality:
    - Stack die to multiply the available memory.
    - Increase functionality by including logic or different types of memory.

Multi-die Package



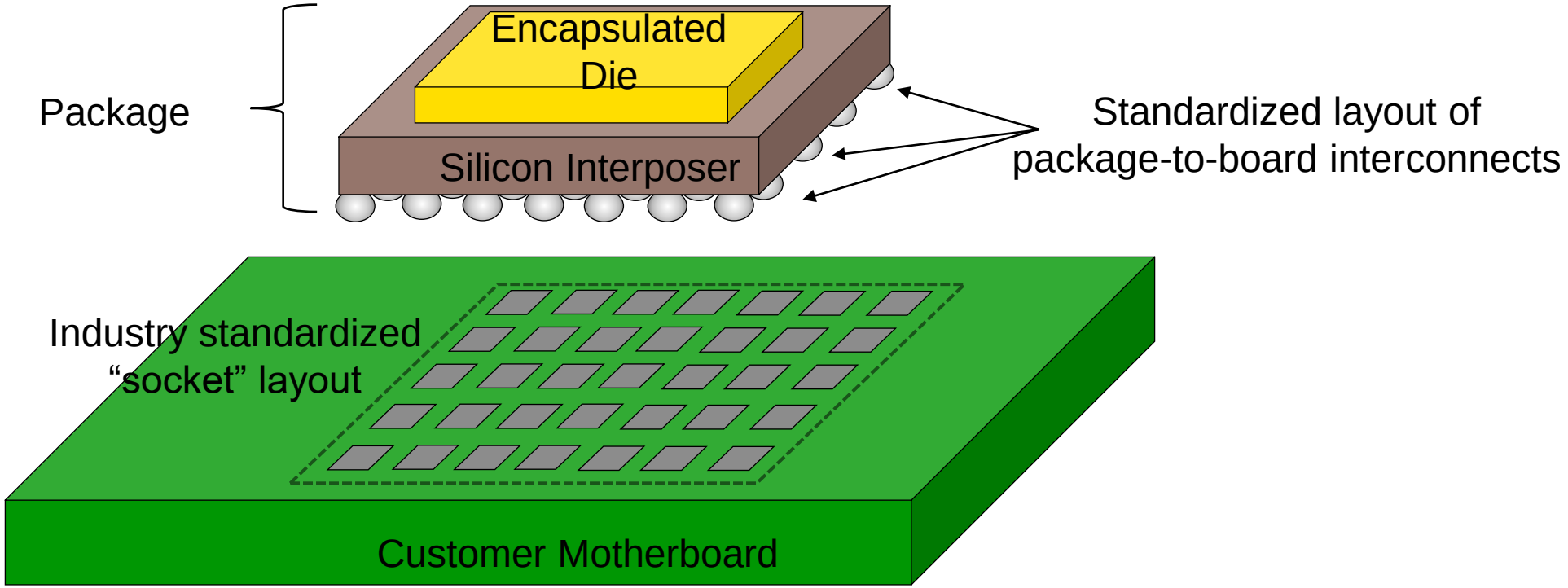
Hybrid Memory



Introduction to Packaging

What purpose does the package serve?

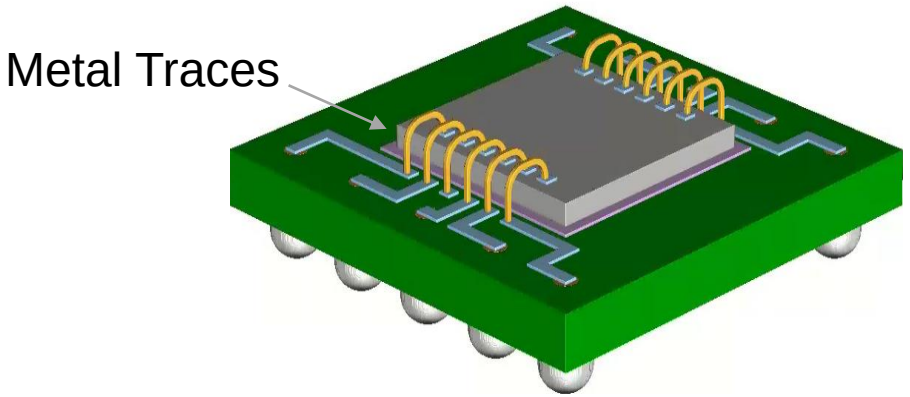
5. Customer ease of use:
    - Standardized sockets allow for quick attachment, replacement, or upgrade of products.



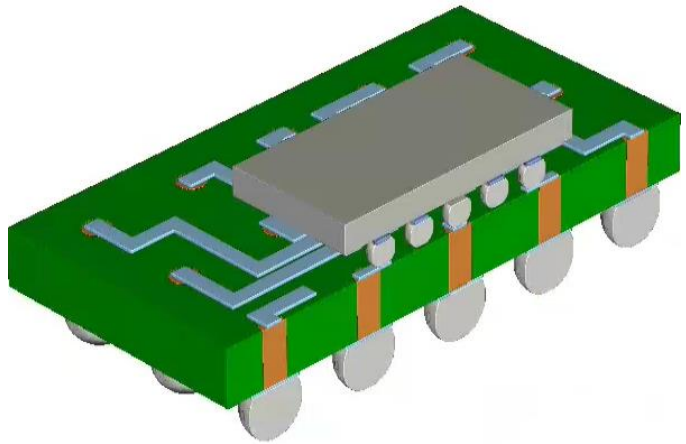
Introduction to Packaging

In the process of fabricating die, chemical and laser etchings expose connections on the top of die. To make an electrical connection, wires can be bonded to these connections on the top, or the die can be inverted (“flipped”) to apply bonds to the bottom.

Wire bond: Very thin wires (usually gold) connect bond pads on the die to metal traces on the interposer. Over 80% of integrated circuits use wire bond.



Flip Chip: Die is inverted. Solder balls on the die are directly bonded to metal pads on the package substrate.

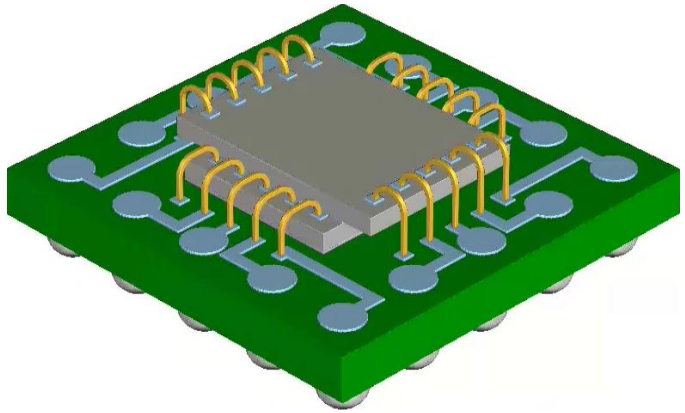


Wirebonded Package

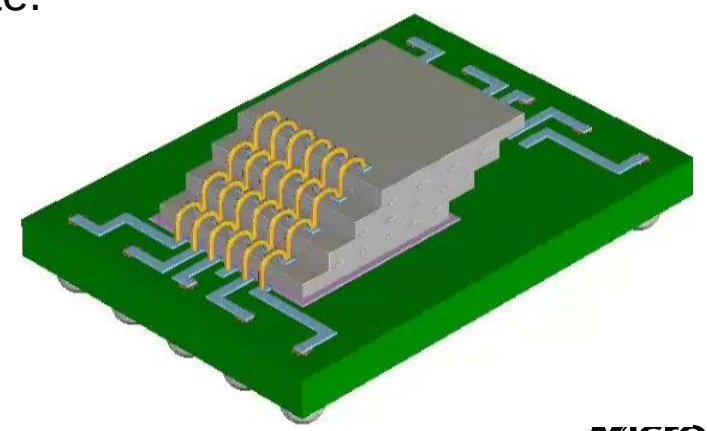
Utilize wires bonded to pads on the top of the die down to pads on the substrate.

- Cheaper, easier fabrication process.
- Adaptable to different chip sizes and other package design considerations.
- Requires a larger overall package.
- Long wires result in greater parasitic voltage loss, slower signal transmission.

Wire bond – Direct: Wire bond is used to connect each die directly to the assembly substrate.



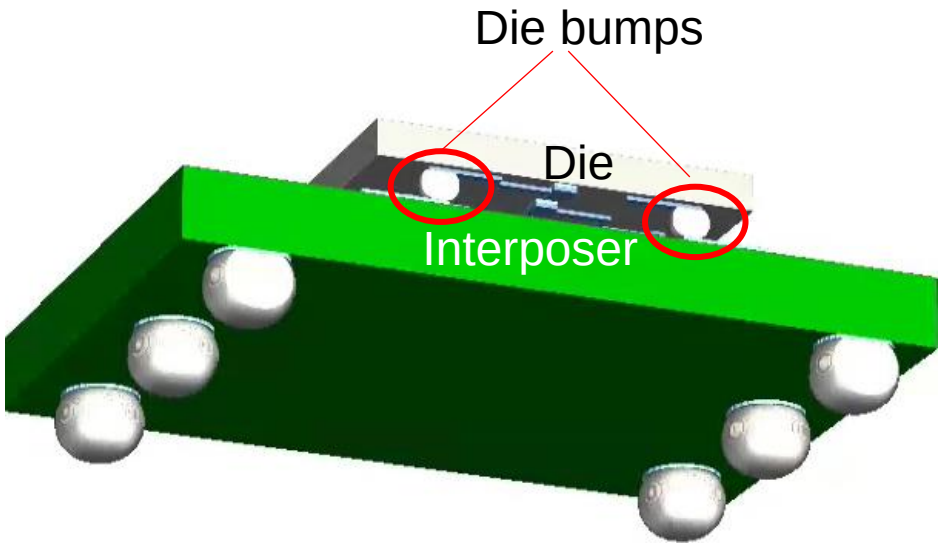
Wire bond - Cascading: Wire bonds cascade from one die to the next, ending at the substrate.

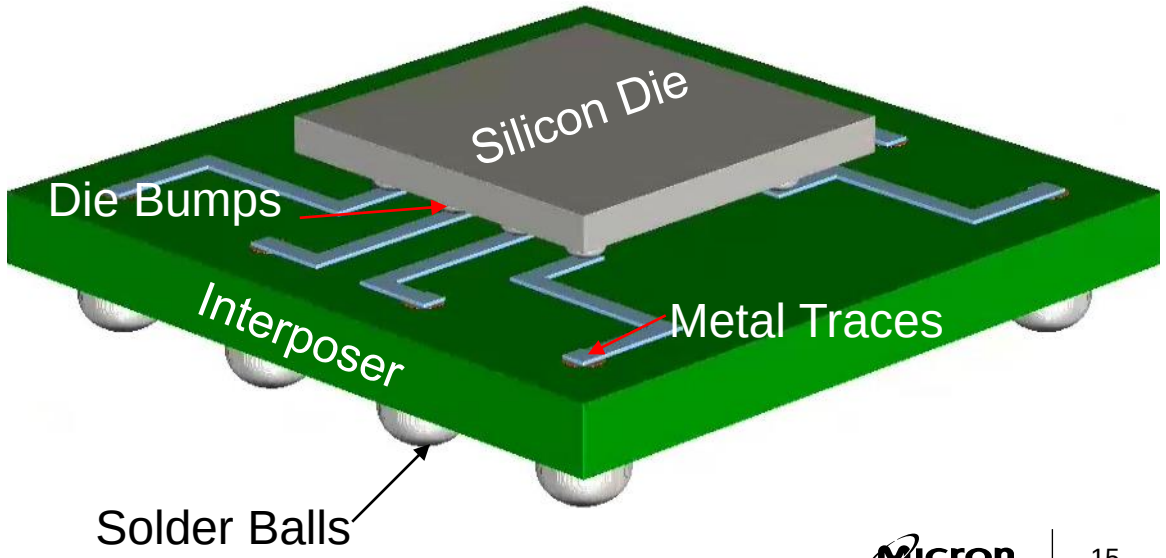


Bumped Package

Solder ball “bumps” make electrical connections between metal pads on bonding surfaces.

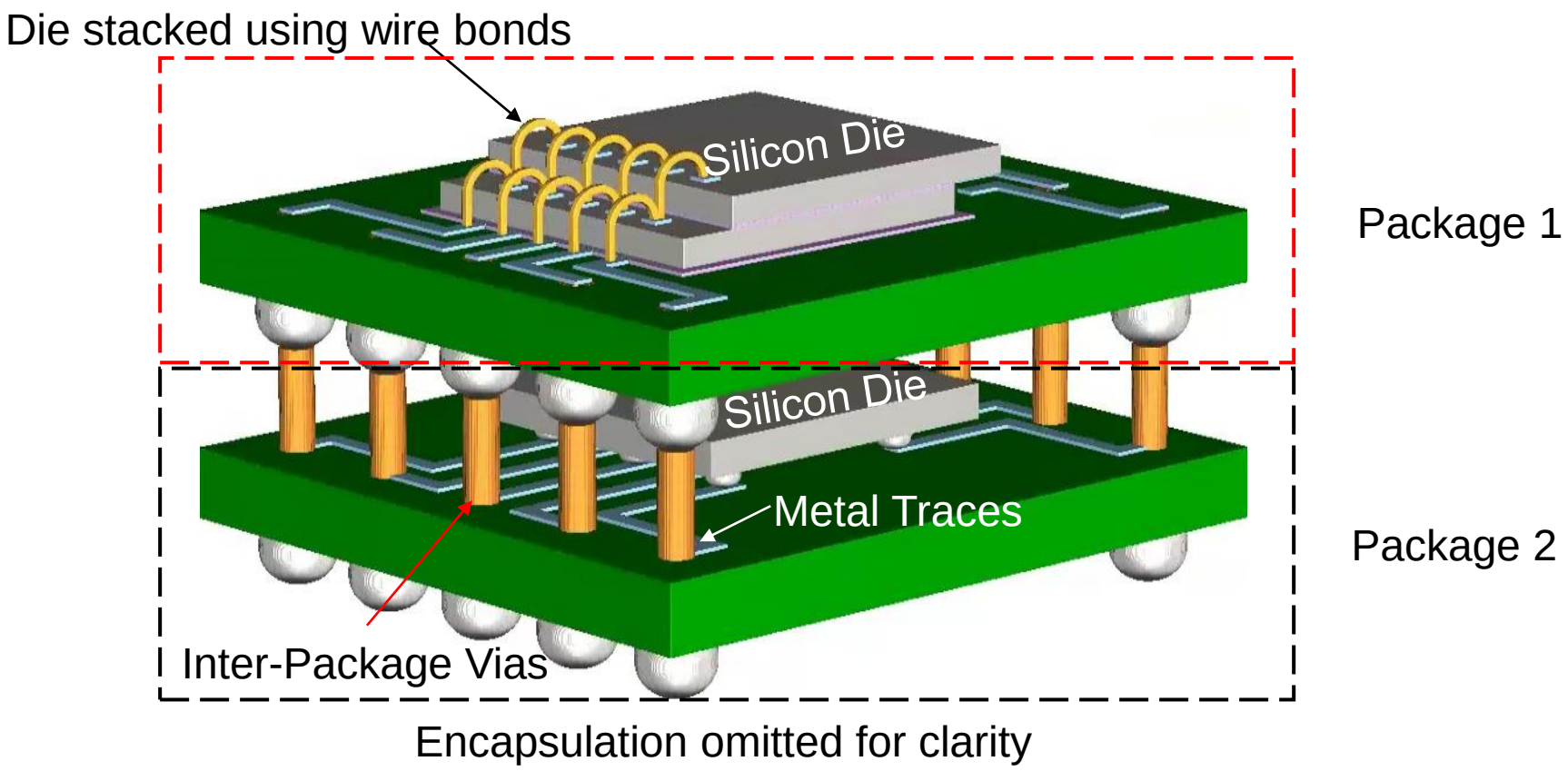
- More complex fabrication process, increased cost compared to wire bonds.
- Changes to chip size and other package designs often require re-designing the bonding pattern.
- Small electrical connections result in far lower parasitic voltage loss.
- Enables high density interconnects and shrinks overall package size.





Package-on-Package

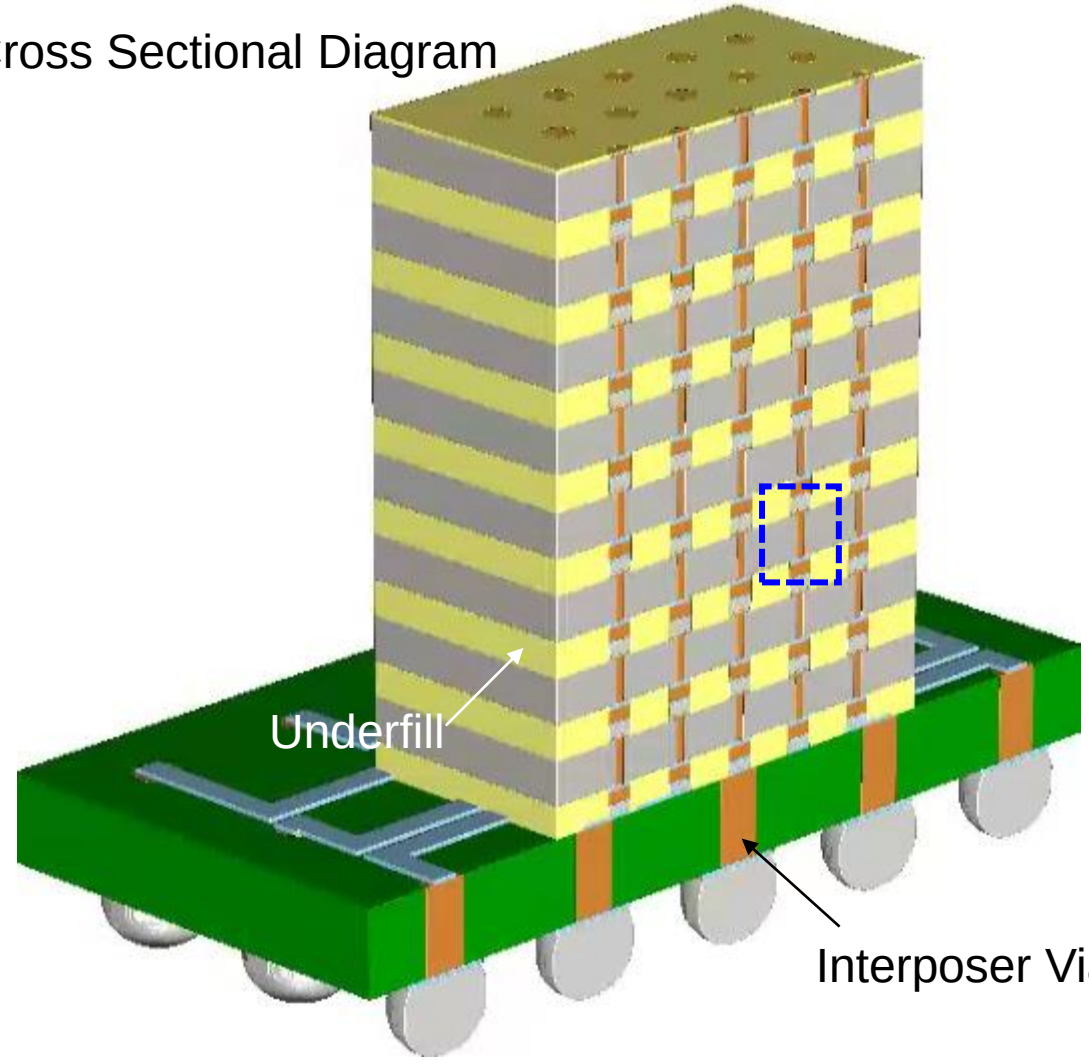
“Bumped” die are not easily stacked. Can expand memory then by stacking entire packages. Enables blended bonding types as well.

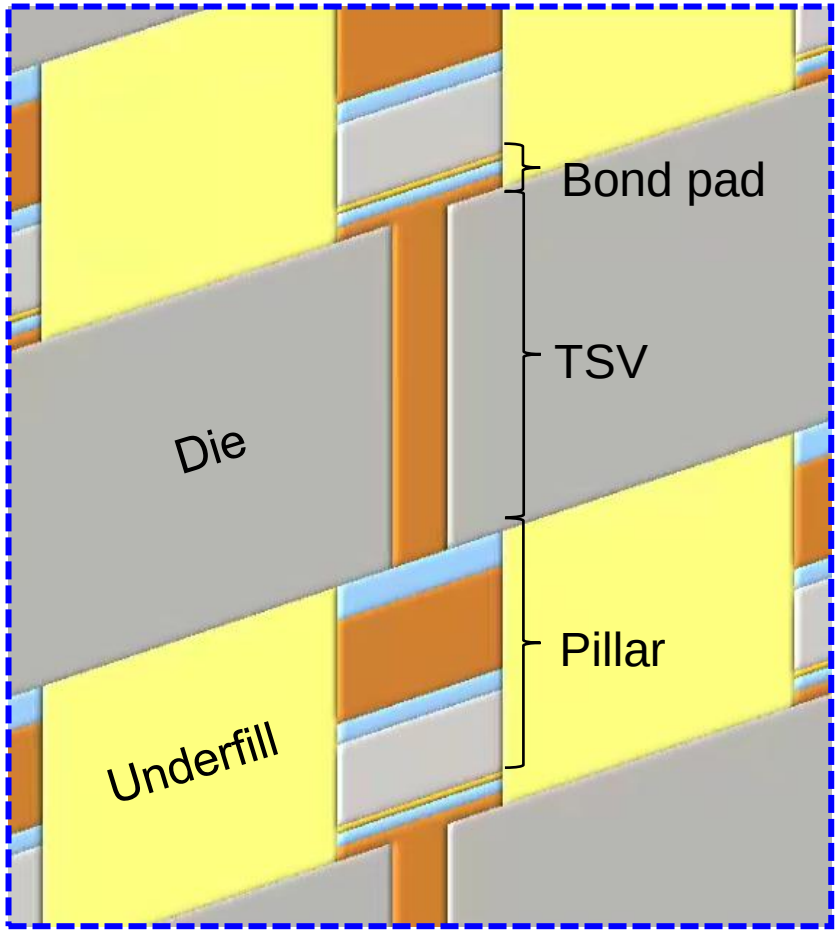


Through Silicon Vias (TSV's)

Newer fabrication technique runs metal pillars or "vias" through the thickness of the die. Electrically connects the die and bonds to the interposer.

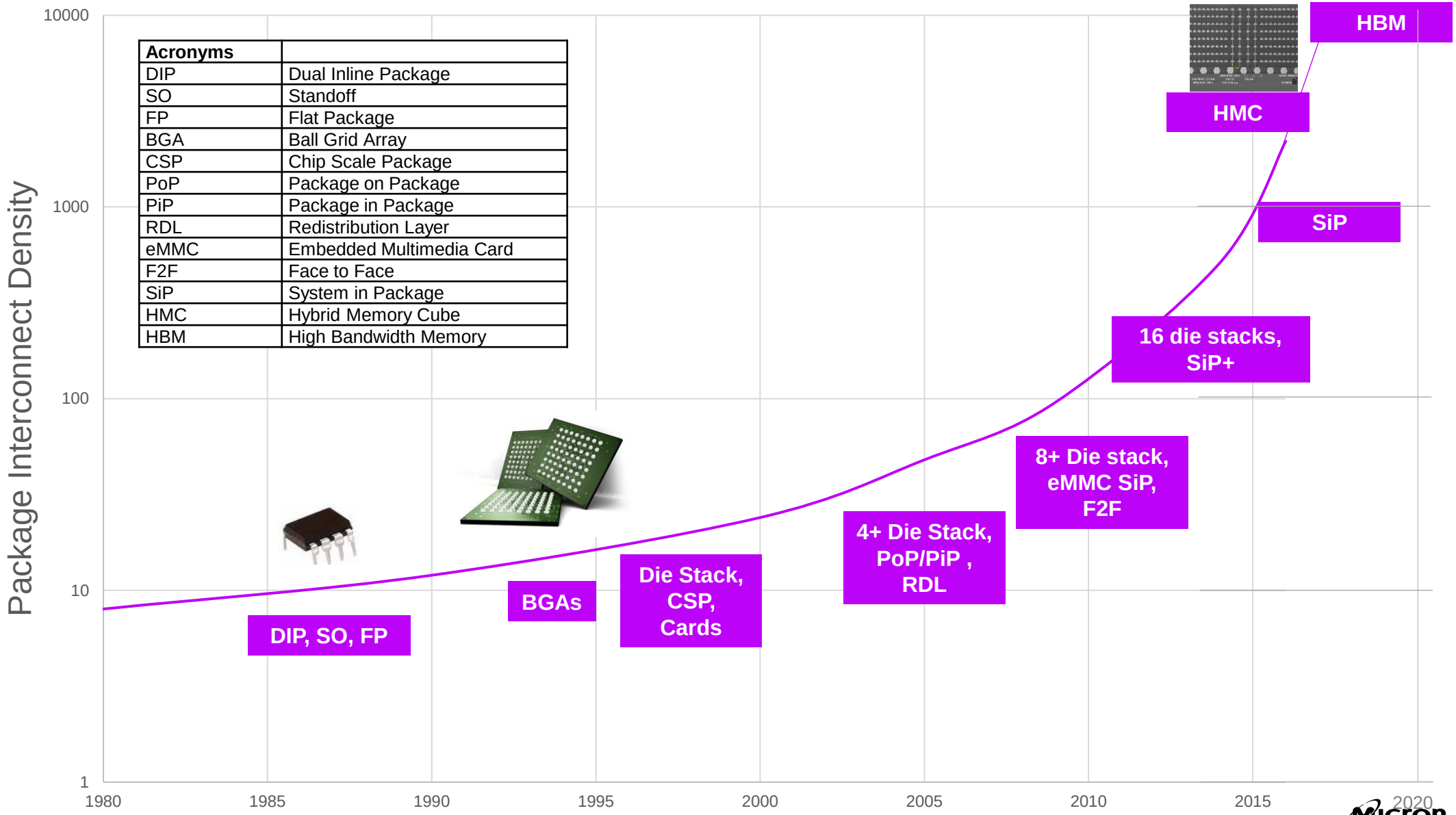
Cross Sectional Diagram





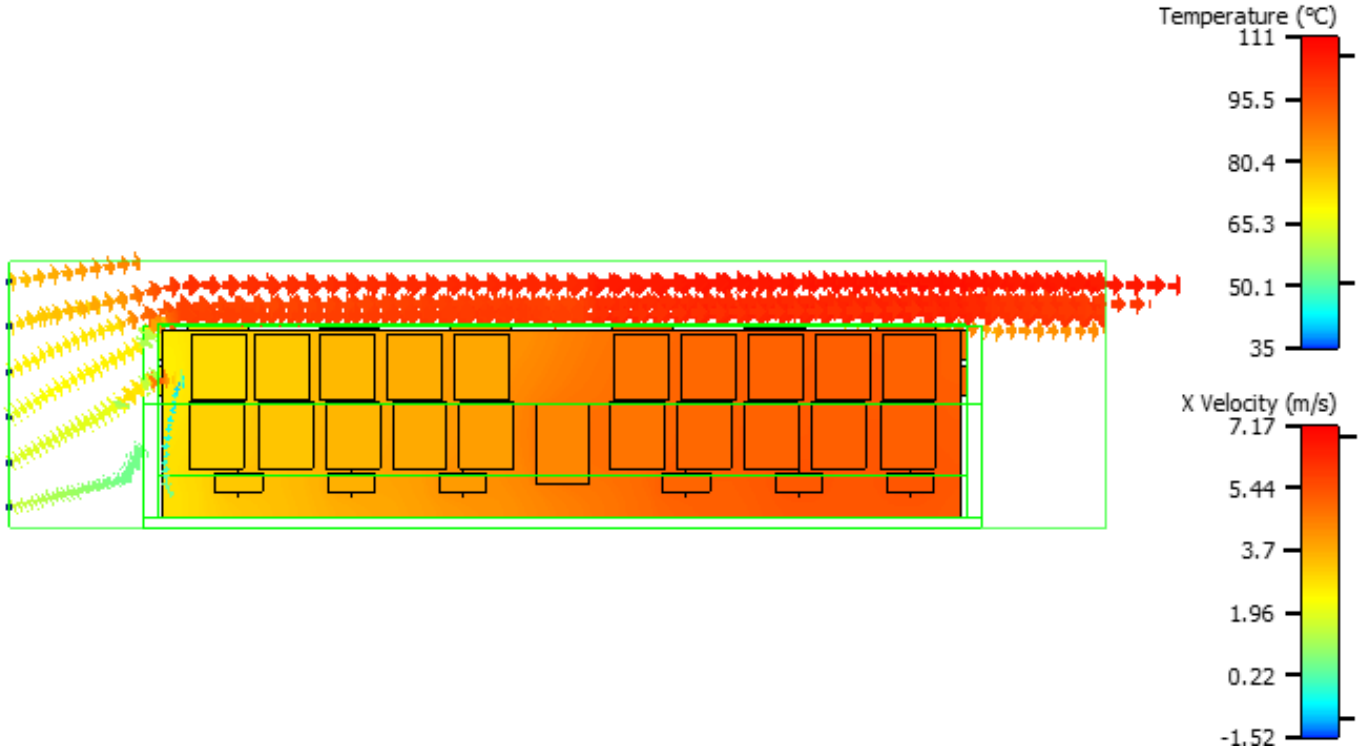
Challenges in Packaging: Scaling!

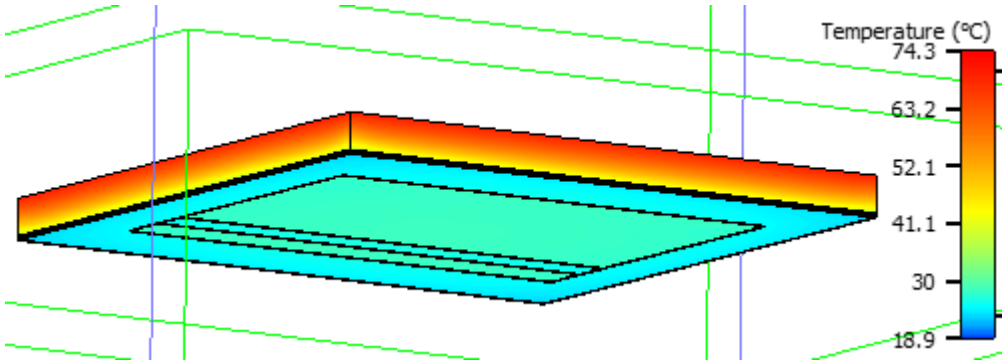
Acronyms	
DIP	Dual Inline Package
SO	Standoff
FP	Flat Package
BGA	Ball Grid Array
CSP	Chip Scale Package
PoP	Package on Package
PiP	Package in Package
RDL	Redistribution Layer
eMMC	Embedded Multimedia Card
F2F	Face to Face
SiP	System in Package
HMC	Hybrid Memory Cube
HBM	High Bandwidth Memory



Thermal Simulation

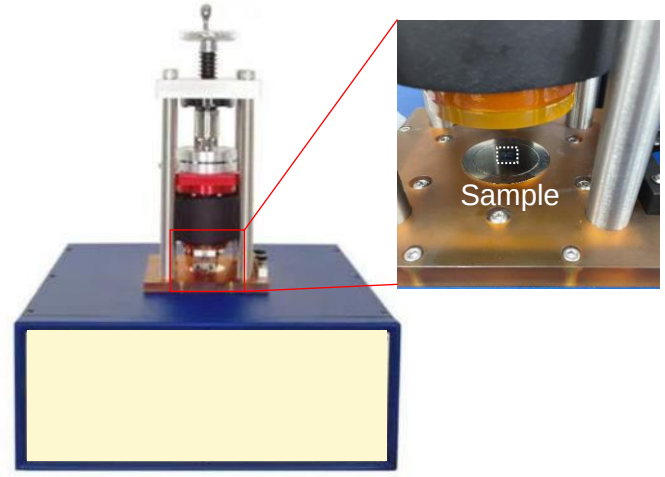
Thermal modeling is a powerful tool for predicting how packages will perform while in different situations.

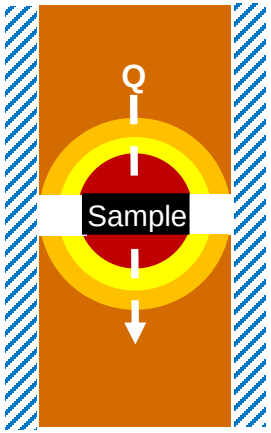




Laboratory Testing

Computer simulations require comparison to experimental data for validation.



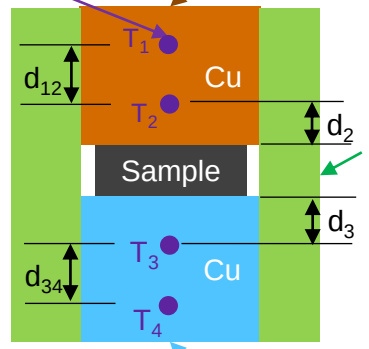


Four locations
In Cu blocks

Heat Source
Power (P)

$$T_T = T_2 - \frac{d_2}{d_{12}}(T_1 - T_2)$$

$$T_B = T_3 + \frac{d_3}{d_{34}}(T_3 - T_4)$$



Insulators

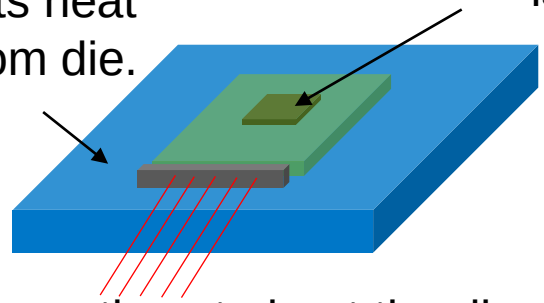
Isothermal
Heat sink: 0°C

$$\theta_{TB} = \frac{(T_T - T_B)}{P}$$

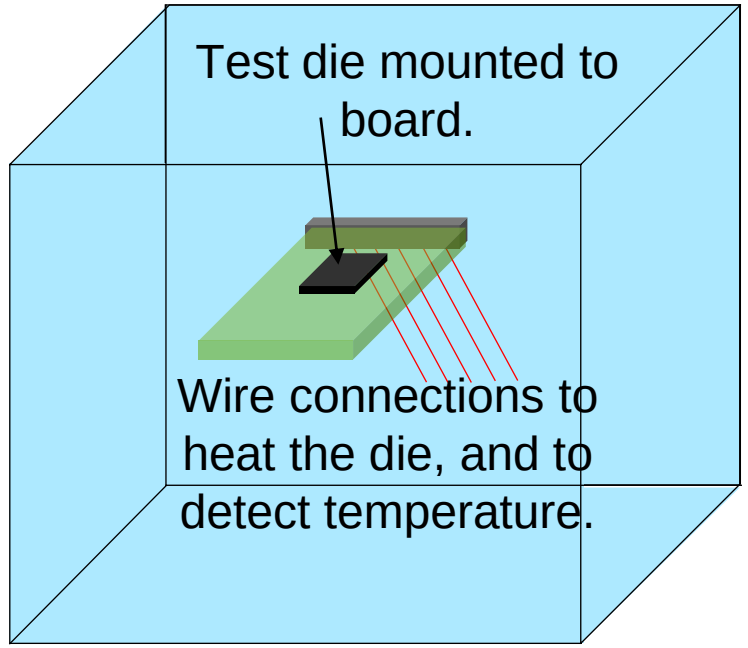
Laboratory Testing Environments

Cold plate (20 C). Conducts heat away from die.

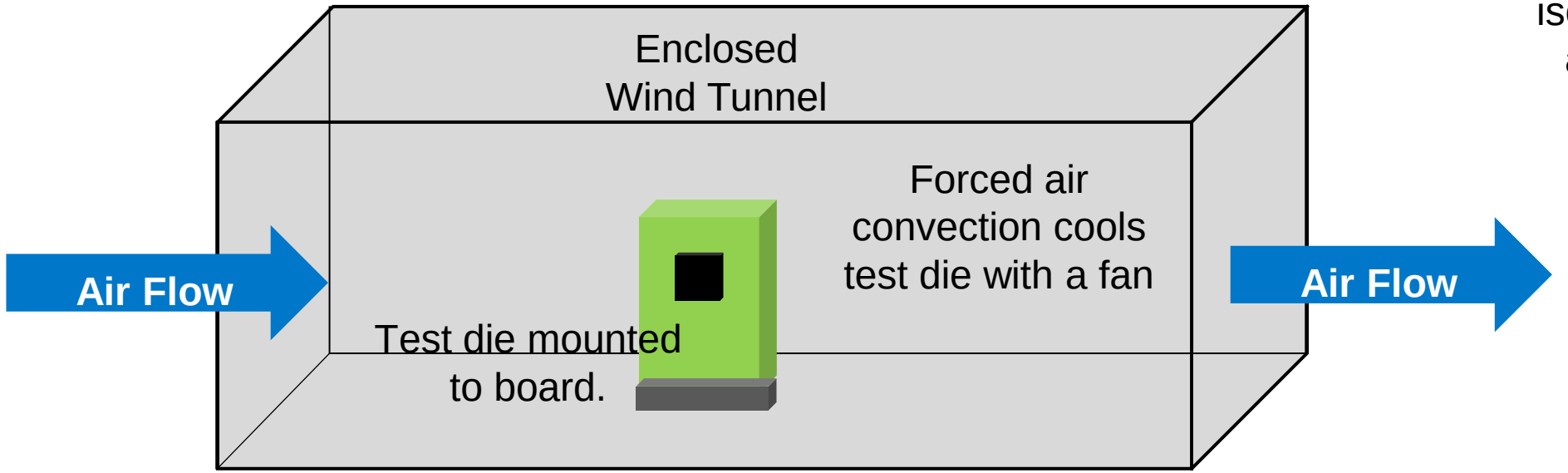
Test die mounted to board. Die is in contact with cold plate.



Wire connections to heat the die, and to detect temperature.



Acrylic chamber to isolate test die from ambient air flow.



Mechanical assessment

Computer simulations are also used to evaluate mechanical behaviors like warpage and contact.

Engineering Disciplines in Packaging

Tackling challenges in packaging requires a diverse educational background

- Mechanical Engineering: Evaluate package warpage, mechanical integrity, thermal characterization.
- Electrical Engineering: Design and evaluate electrical routing of die and interposers in the package.
- Materials Science: Chemistry, metallurgy, and innovations in material science drive many of the advancements in semiconductor technology.
- Industrial Engineering: Evaluating, procuring, and integrating new tools and processes to enable tighter tolerance manufacturing at continually shrinking scales.

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