Educator Hub

Introduction to Fabrication

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Agenda

1 Introduction to Fabrication

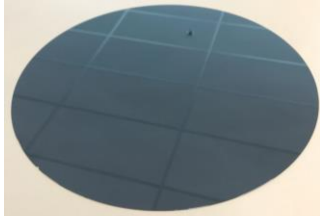
2 Basic CMOS Process Flow (Traveler)

1) Introduction to Fabrication

Fabrication

Fabrication is the process of building circuits on a silicon wafer in a **cleanroom** environment where all aspects of production (temperature, power, chemistries, moisture, contamination, etc.) are tightly controlled.

Silicon wafers are purchased from Vendors

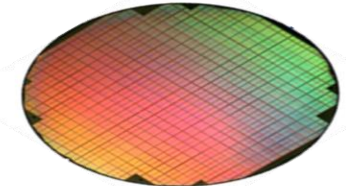


Bare silicon 300mm wafer

Fabrication or Manufacturing

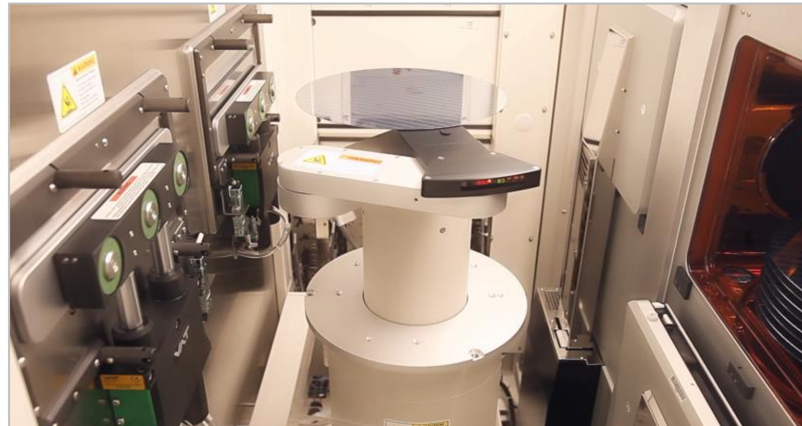
How long does it take to complete fabrication?

(45-140 days)

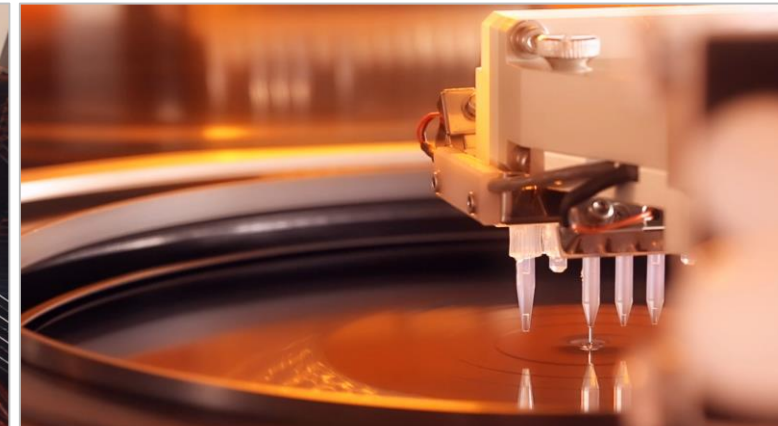


Completed wafer ready for Probe and Final Parametric testing

Picture inside a cleanroom fab



Picture inside a tool: robot that handles wafers



Picture inside a tool: dispensing photoresist in a photolithography tool

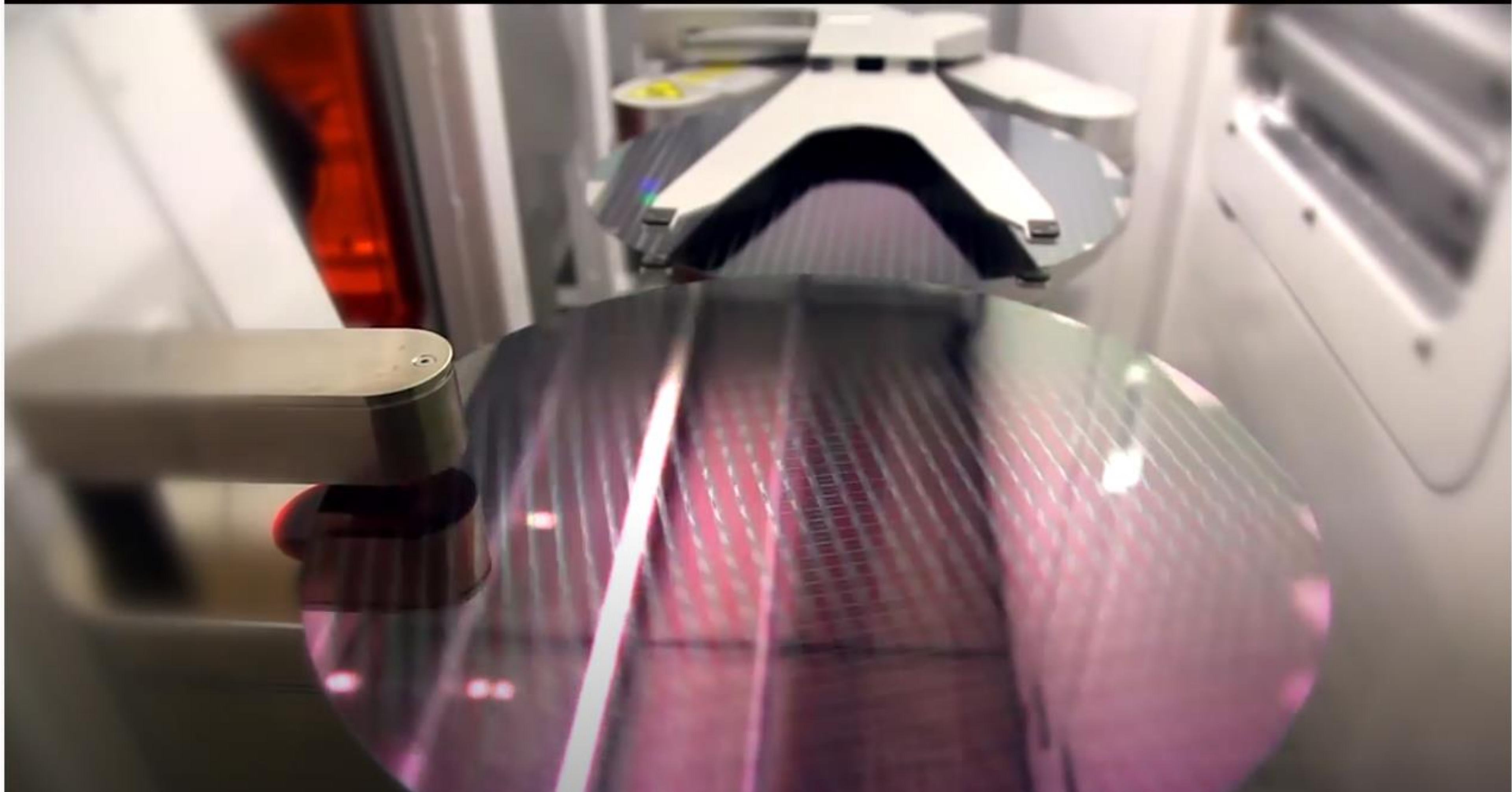
Fabrication Facilities are Cleanrooms

View of the fab from the ceiling, on the path of the AMHS (Automated Material Handling System)

There are hundreds of tools in a semiconductor fab

View of a tool in a fab

Automation inside a tool



Picture inside a tool: robot that handles wafers

Cleanrooms & Classification Standards

Q: What Is a Cleanroom?
A: A cleanroom is a room that has HEPA filtration to remove particles from the air. Cleanrooms are used for manufacturing where high levels of cleanliness and sterility are required. Common applications are medical devices, pharmaceutical and **semiconductor manufacturing**.

Note: US Fed standard in particles per ft^3 superseded in 2021 by ISO standard using particles per m^3.

ISO 14644-1 Cleanroom Standards							
ISO Class	Maximum Particles per m^3						FED Standard
	≥0.1µ	≥0.2µ	≥0.3µ	≥0.5µ	≥1µ	≥5µ	
ISO 4	10,000	2,370	1,020	352	83		Class 10
ISO 5	100,000	23,700	10,200	3,520	832	29	Class 100

Question: Why do we wear smocks in the fab?

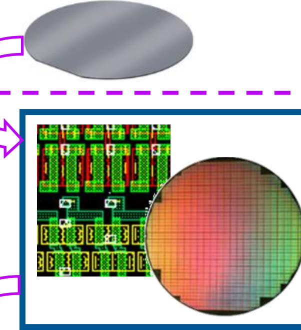
To protect wafers from human and other contamination

Semiconductor Memory Manufacturing Flow

Start Material: Silicon is purified and formed into wafers (outside Micron).

This document focuses on this part

Wafer-Level Fabrication: Electronic devices (transistors, resistors, capacitors, etc.) are fabricated on the silicon wafers, and are then interconnected together into complete circuits.



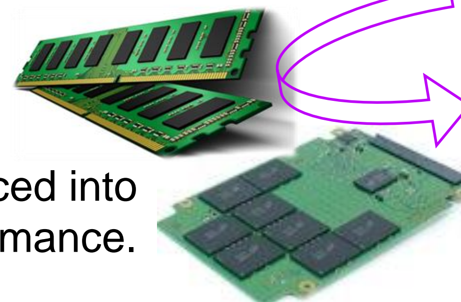
Probe: Each die is tested for functionality, failing die are flagged. Failure data (bins) is collected for yield improvement.

Param: Wafer-level electrical data is collected to characterize and improve the process.

Packaging: Die that pass Probe are separated from the wafer and assembled into packages.

Final Test and Burn-In: Packaged parts are tested for functionality. Some parts are given additional tests under harsh conditions to verify reliability.

Module Assembly and Testing: Some DRAM Packaged parts are placed into Modules and further tested for functionality and reliability.



System/SSD Testing: NAND packaged parts may be placed into SSDs or Composite drives and further tested for performance.

Customer!

Wafer Processing Areas – Five Basic Actions

1. **Creating Patterns**
   Photolithography

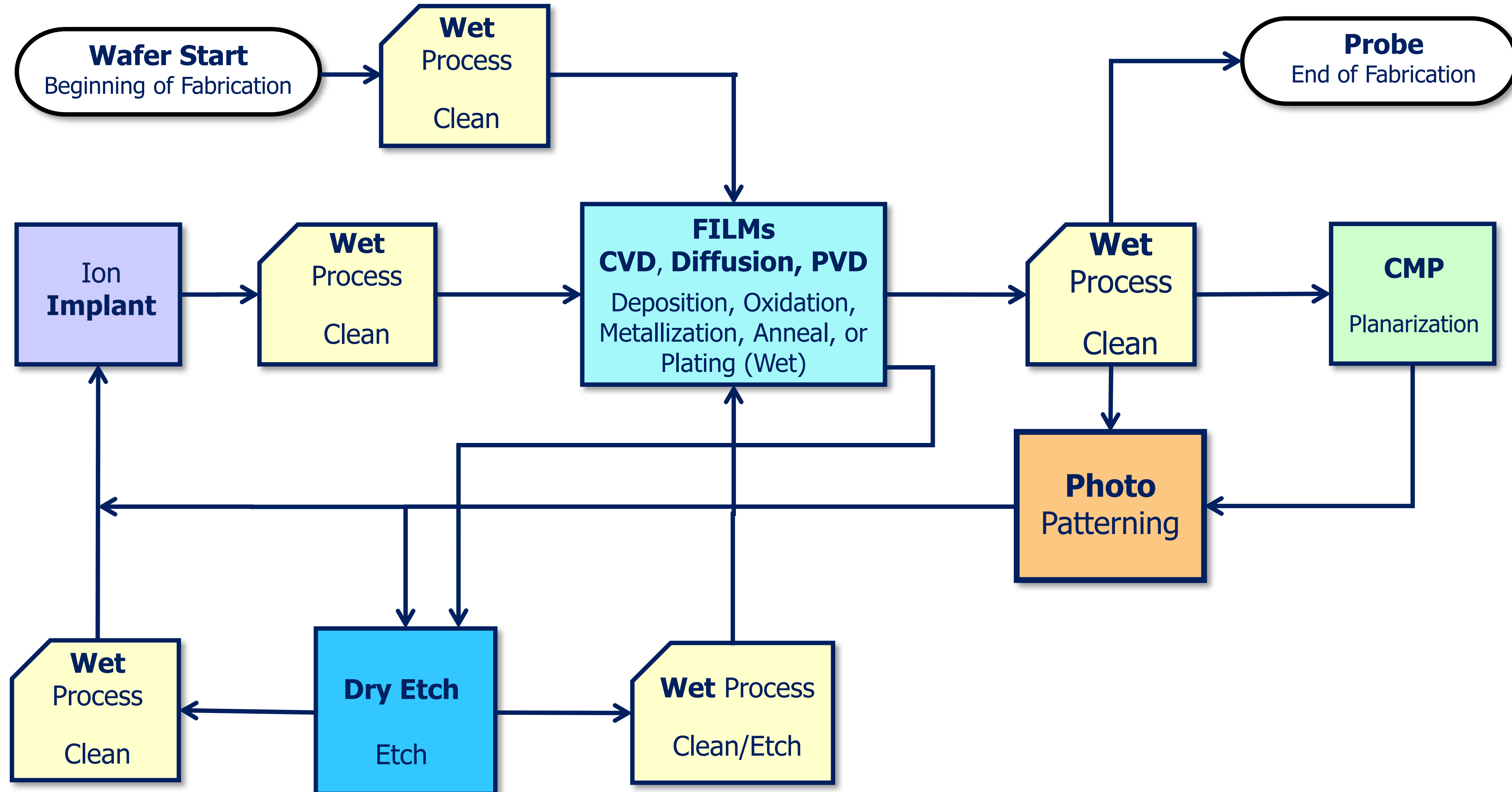
2. **Changing electrical properties**
   Implant

3. **Removing/Etching Material**
   Dry Etch
   Wet Process
   CMP (chemical mechanical planarization)

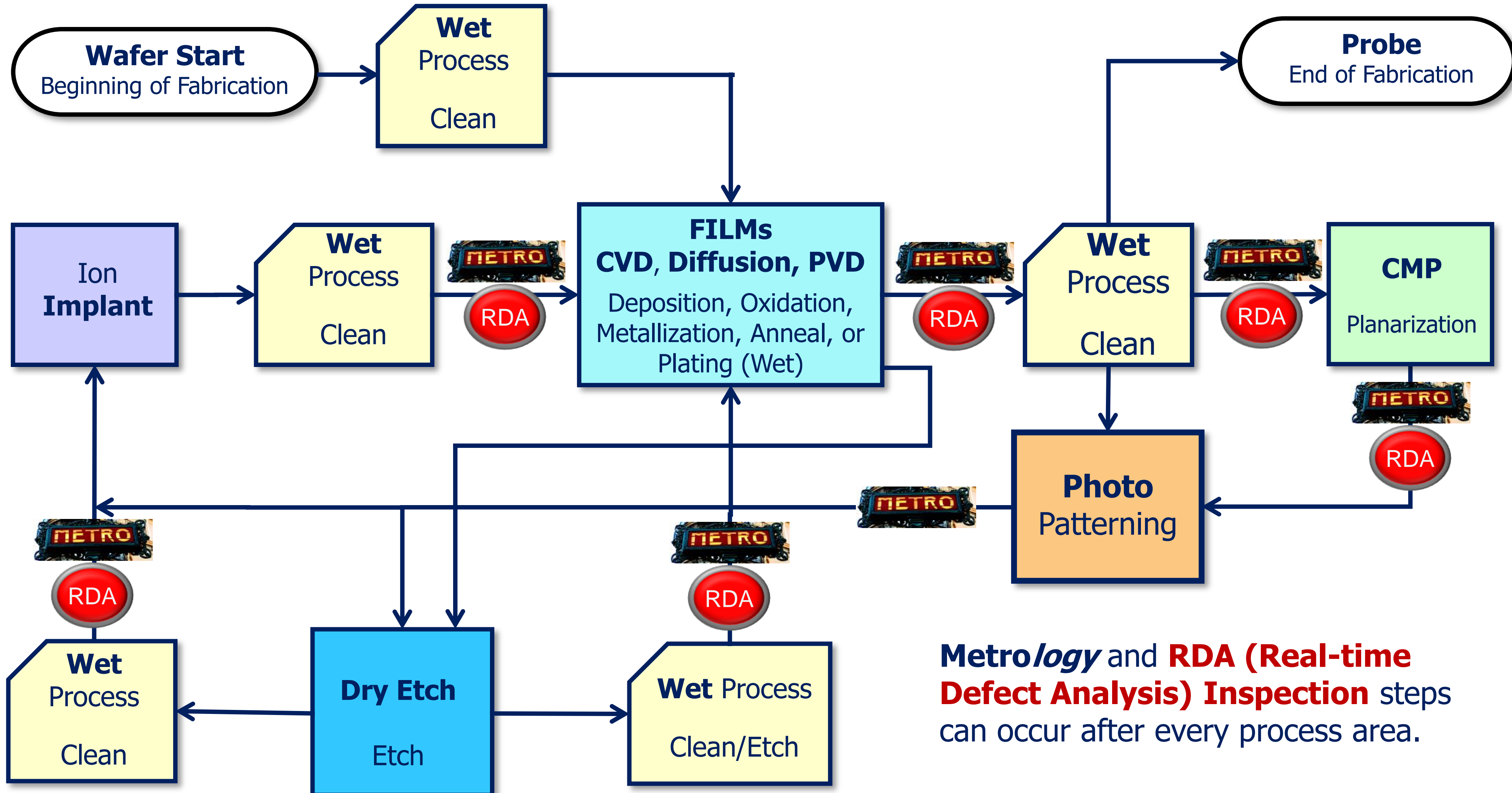
4. **Adding Material**
   Diffusion
   CVD (chemical vapor deposition)
   PVD (physical vapor deposition)
   Wet Process (electroplating)

5. **Measuring/Inspecting**
   Metrology
   RDA (real-time defect analysis)

Simplified Wafer Processing Flow



Simplified Wafer Processing Flow



Metro*logy* and **RDA (Real-time Defect Analysis) Inspection** steps can occur after every process area.

Wafer Process Traveler

A **Traveler** is the list, in order, of every step needed to make a memory chip. Years ago it was printed on cleanroom paper and "traveled" along with the box of wafers. Nowadays tracking is all performed online.

A Traveler may have more than a thousand steps!

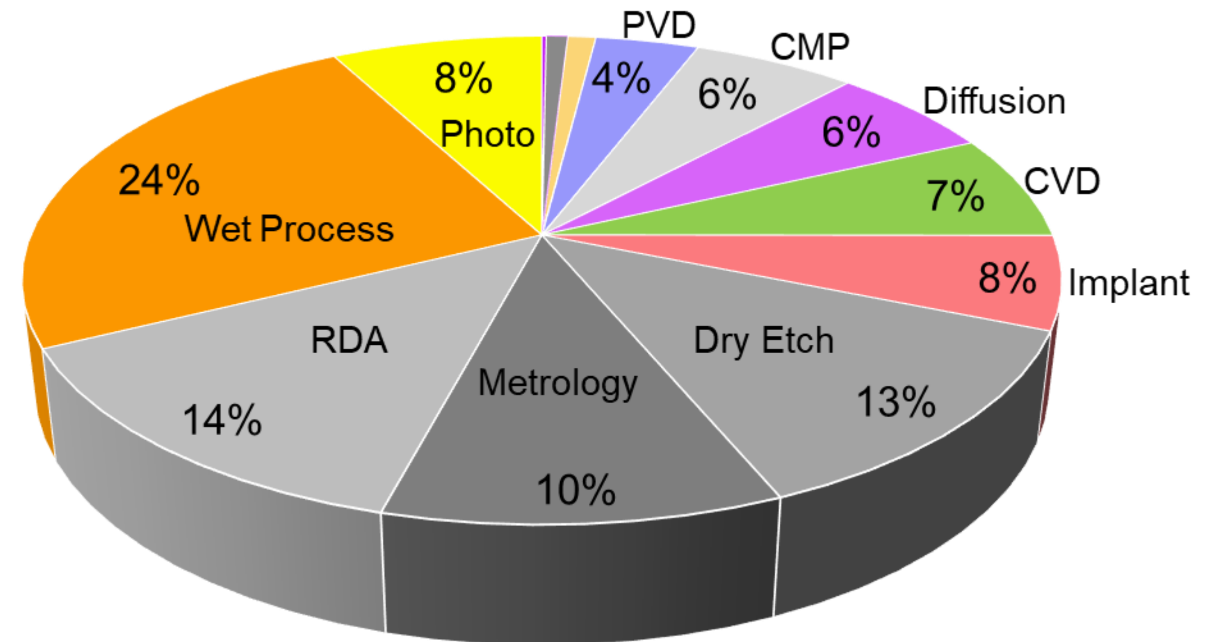
Each Traveler step belongs to one of the 10 Fab areas.

Each Traveler step has a **Recipe** associated with it. The Recipe contains detailed instructions to process the wafer (for example: temperature, pressure, chemicals or gases used, dilution of chemicals, amount of time, etc.)

Step #	Traveler Step	Area
161	TG - GATE HARDMASK DEPOSITION	CVD
162	TG - GATE PHOTO PATTERN	PHOTO
163	TG - GATE PHOTO ALIGNMENT	METROLOGY
164	TG - GATE CRITICAL DIMENSION	METROLOGY
165	TG - GATE DRY ETCH	DRY ETCH
166	TG - GATE DRY STRIP	WET PROCESS
167	TG - GATE WET CLEAN	WET PROCESS
168	TG - GATE CRITICAL DIMENSION	METROLOGY
169	TG - GATE STRESS	METROLOGY
170	TG - GATE PROFILE	METROLOGY
171	TG - GATE INSPECTION	RDA
172	TG - GATE SPACER WET CLEAN	WET PROCESS
173	TG - GATE SPACER OXIDE DEPOSITION	CVD
174	TG - GATE SPACER OXIDE DRY ETCH	DRY ETCH
175	TG - GATE SPACER OXIDE WET CLEAN	WET PROCESS
176	TG - GATE SPACER CRITICAL DIMENSION	METROLOGY

Breakout of Steps by Functional Area

- There are 10 primary “functional areas” of the fab:
  - **CMP**: Chemical Mechanical Planarization
  - **CVD**: Chemical Vapor Deposition
  - **Diffusion**
  - **Dry Etch**
  - **Implant**
  - **Metrology**
  - **Photo**
  - **PVD**: Physical Vapor Deposition
  - **RDA**: Real time Defect Analysis
  - **Wet Process**

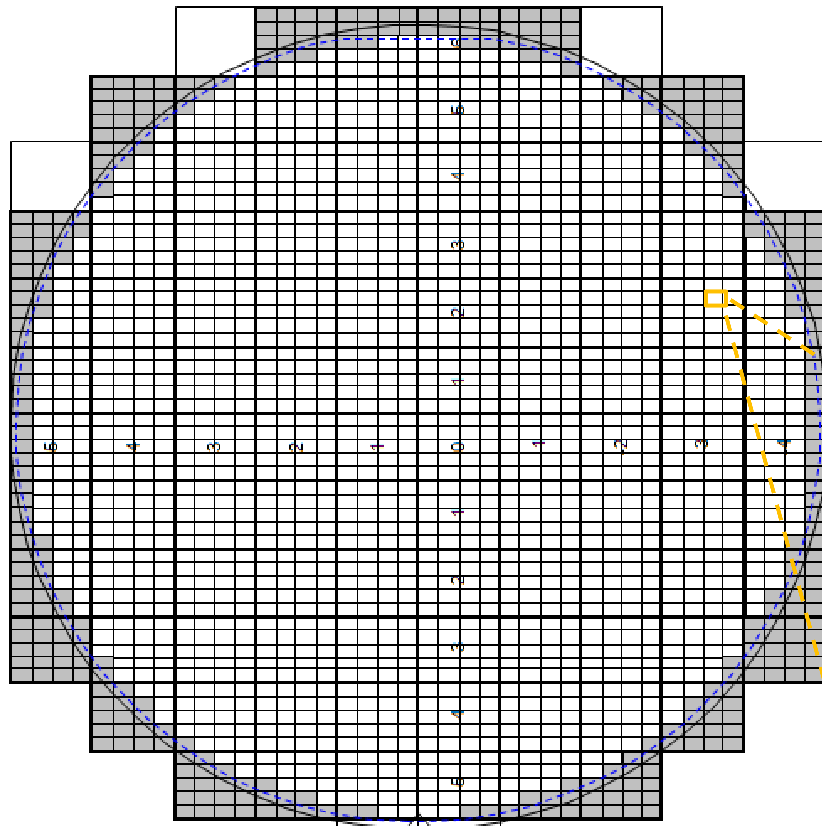


- The pie chart on the right shows a typical distribution of the number of traveler steps by each functional area.

Why do you think Wet Process is the area with the highest percentage of steps?
Hint: look at the slide titled Simplified Wafer Processing Flow

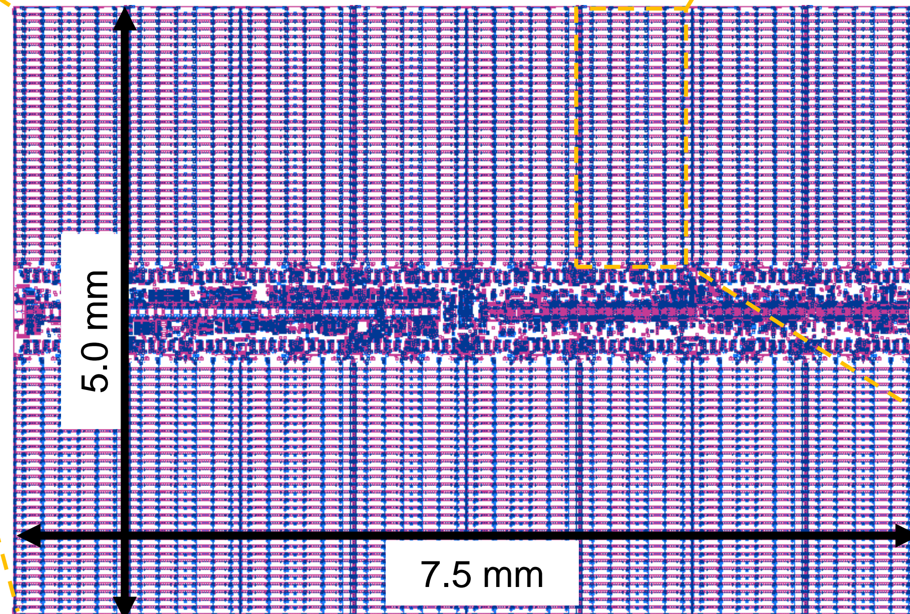
Zoom In to 3D Model

- 3D models are used in this presentation to explain the fabrication process step by step
- These two slides will help to orient the location and scale of the 3D models that are used to describe the traveler flow.

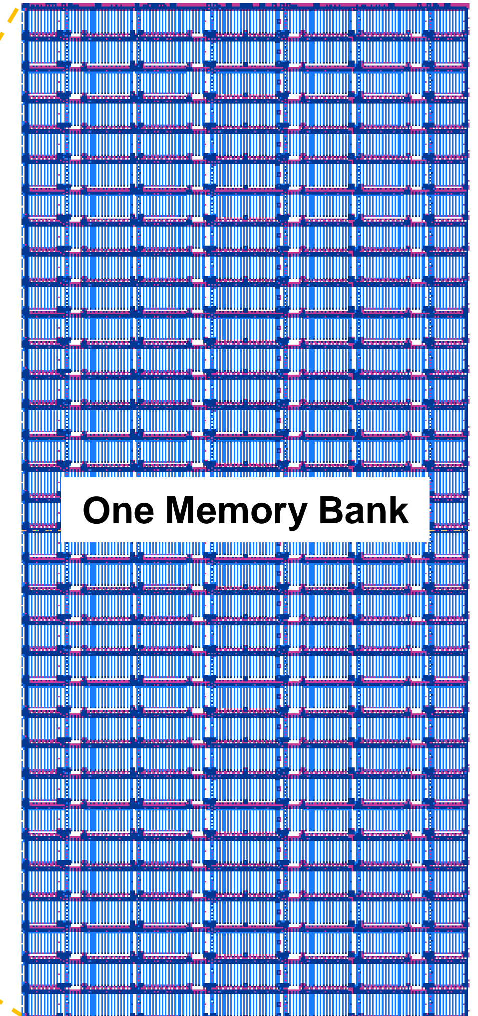


Wafer Map

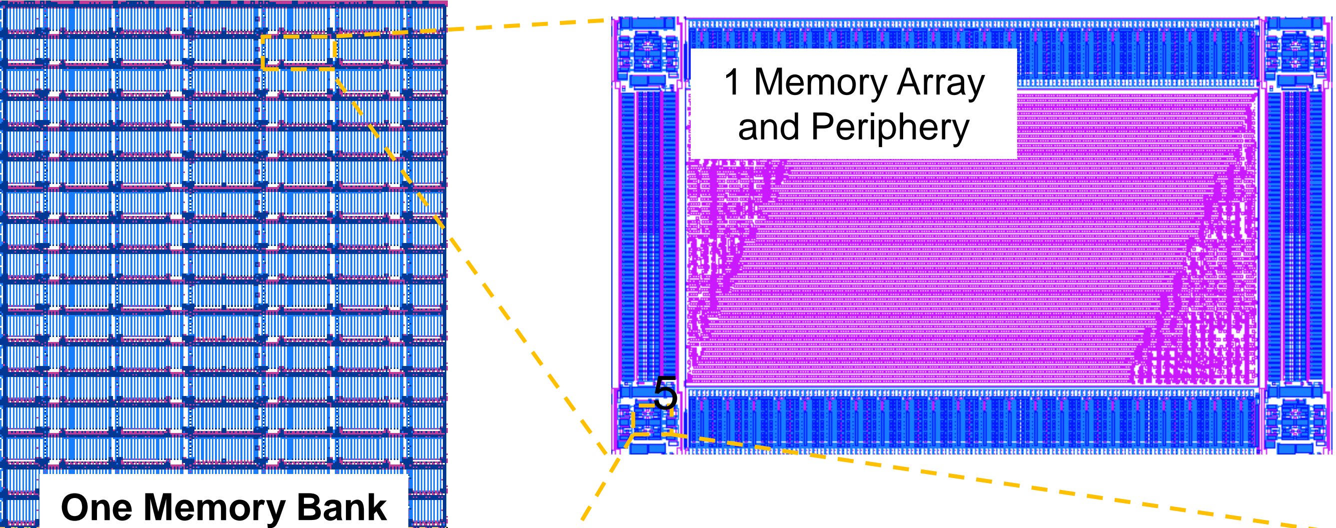
Over 1000 die per wafer

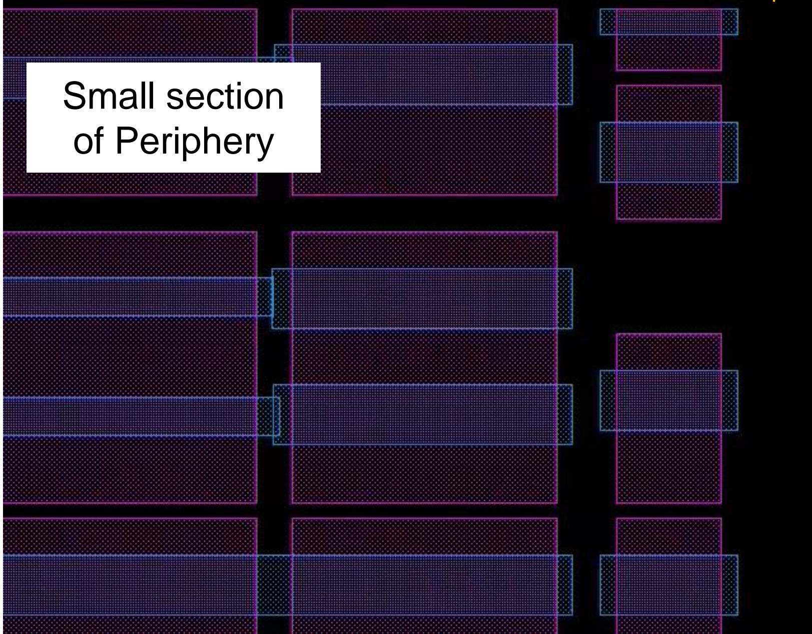


One DRAM Die



Zoom In to 3D Model (continued)





3D Model of a Small
Section of CMOS Periphery

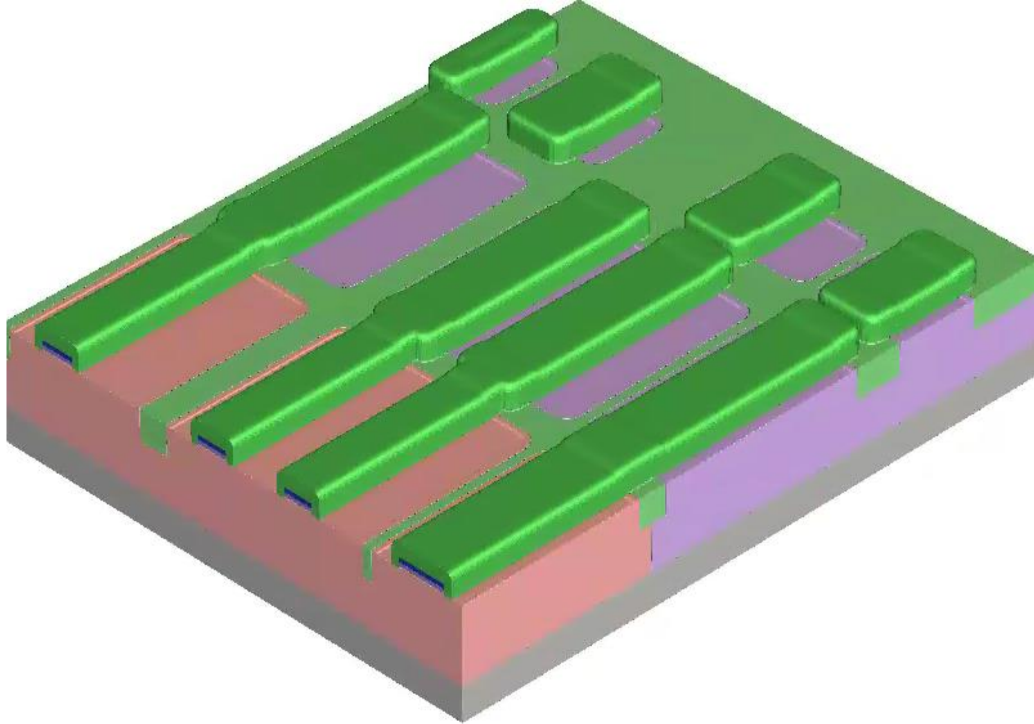


Photo Mask Levels

- During the fabrication process, patterns are created on the wafer using a series of photomasks.
  - Each mask has a unique pattern
  - A typical DRAM or NAND flow may have dozens of different masks
- Micron convention is to assign a 2-digit alphanumeric code to each mask.
- The table below lists the masks that we will use for our simplified CMOS flow.

Code	Description
NW	N-Well (for PMOS devices)
PW	P-Well (for NMOS devices)
AA	Active Areas
TG	Transistor Gates
NA	N-Source/Drain (for NMOS devices)
PA	P-Source/Drain (for PMOS devices)
CN	Contacts (Transistors to Metal1)
M1	Metal1 Interconnects
BP	Passivation and Bond Pads

Basic CMOS Process Flow (Traveler)

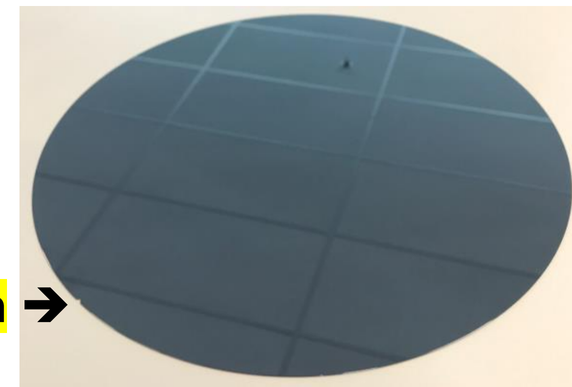
Basic CMOS Traveler

- In the next slides we will show a simplified traveler used to build CMOS transistors (NMOS and PMOS transistors) along with contacts and a metal routing layer.
- As new traveler steps are introduced, we will provide a brief description of the Fab Areas that perform those steps

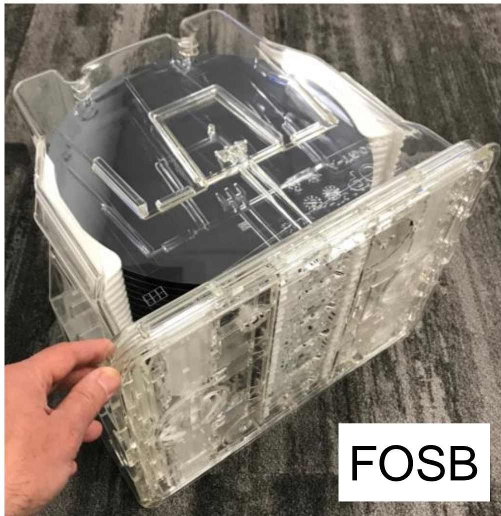
WAFER START with BARE SILICON SUBSTRATE

- Double-side polished bare silicon wafers (with alignment “notch”), also called Silicon Substrates, are received from our external suppliers in 25-wafer Front-Opening Shipping Boxes (FOSB)
  - Wafers are transferred into a Front-Opening Unified Pod (FOUP) in which they will reside as they move from tool to tool during their whole processing “life” within the fab cleanroom
  - Typical Wafer Specs:
    - Thickness = less than 1 mm (3D model only shows top 1µm of Si thickness)
      - Diameter = 300 mm
        - Resistivity = lightly doped P-type

Notch ➔



Grid pattern is reflection of office ceiling 😂



4.5 microns (µ)

Silicon Substrate

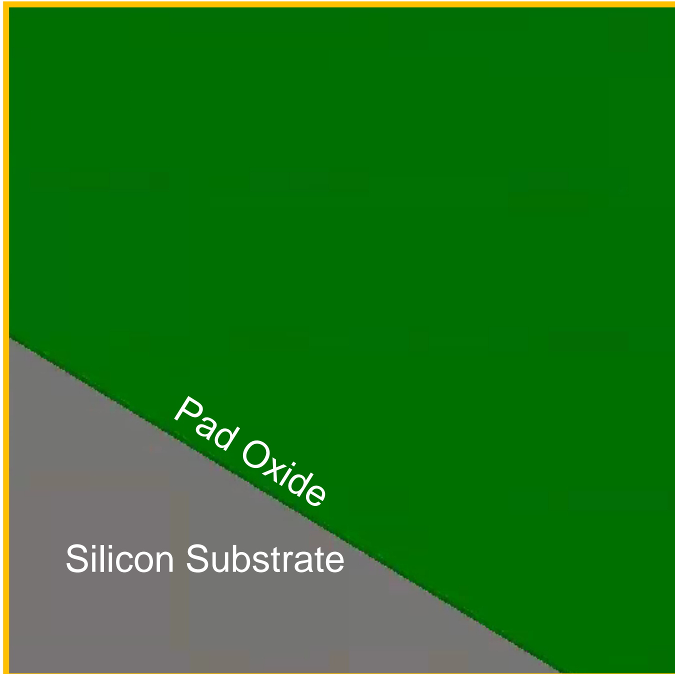
3D Model views are typically only a few microns on a side

…for the record… 300mm is the size of a record

PAD OXIDE GROWTH [DIFFUSION]

- In the **<u>Diffusion Area</u>** a thin film of silicon dioxide is <u>grown</u> on the surface of the wafer to protect the silicon substrate from surface damage during implants and to keep the surface clean and free from defects.
- Silicon dioxide is usually referred as “oxide” and is an insulator or dielectric
- This specific oxide in this location of the traveler is sometimes called “Pad Oxide”

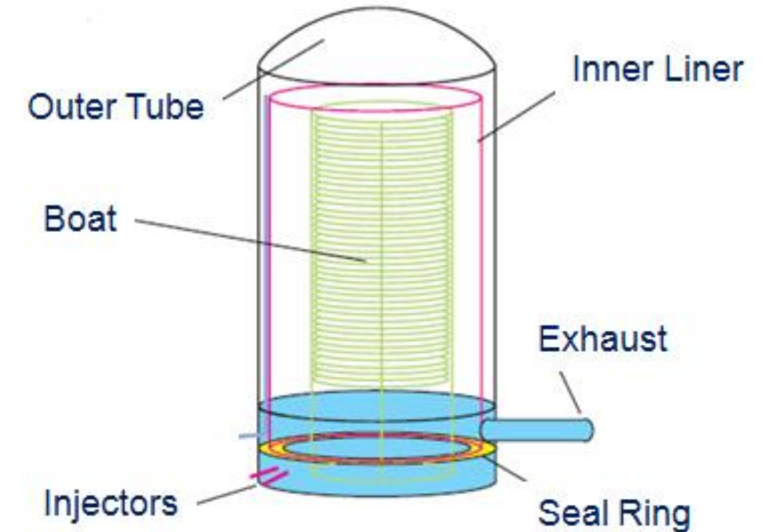
Detail Close-up

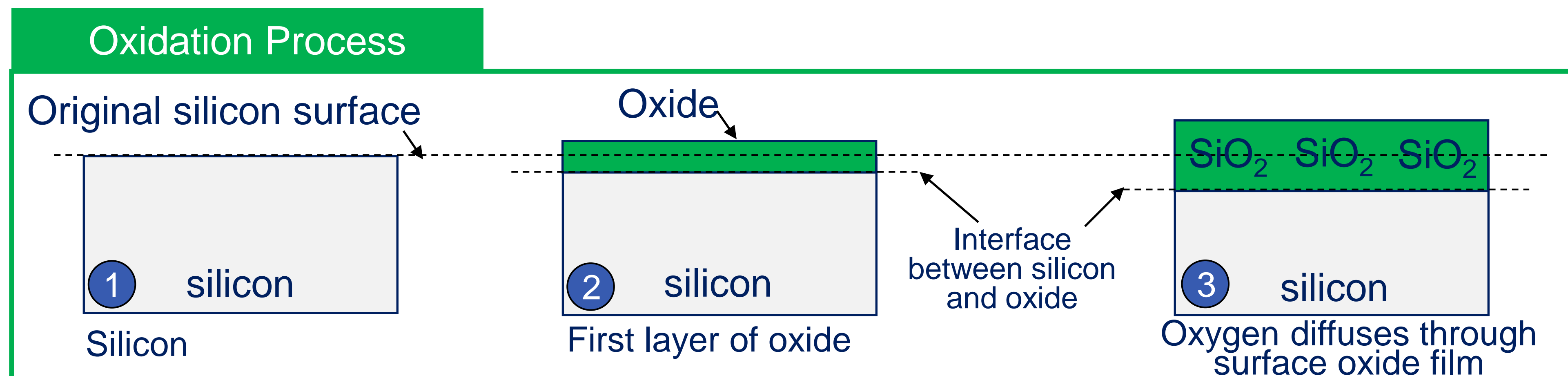


Pad Oxide
Silicon Substrate

Oxidation (Diffusion)

- The Diffusion area of the fab consists primarily of vertical furnace tubes where many wafers can be processed at a time (a batch process – upwards of 125-wafers at a time)
- Many different processes take place in the furnace tubes, including:
  - **Oxidation** – growth of a high-quality silicon dioxide layer on exposed silicon (process shown below)
  - **Deposition** of films (similar to CVD)
  - **Heat treatment** – needed to repair damage or achieve certain electrical results

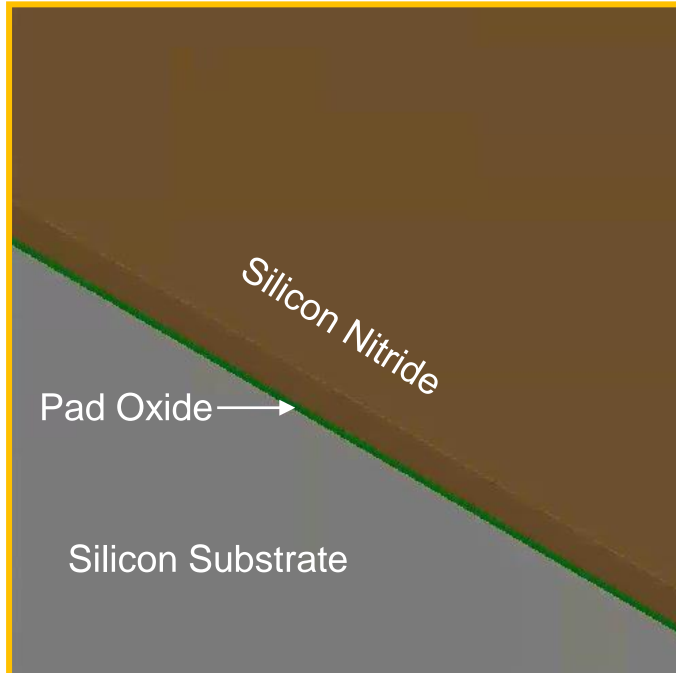




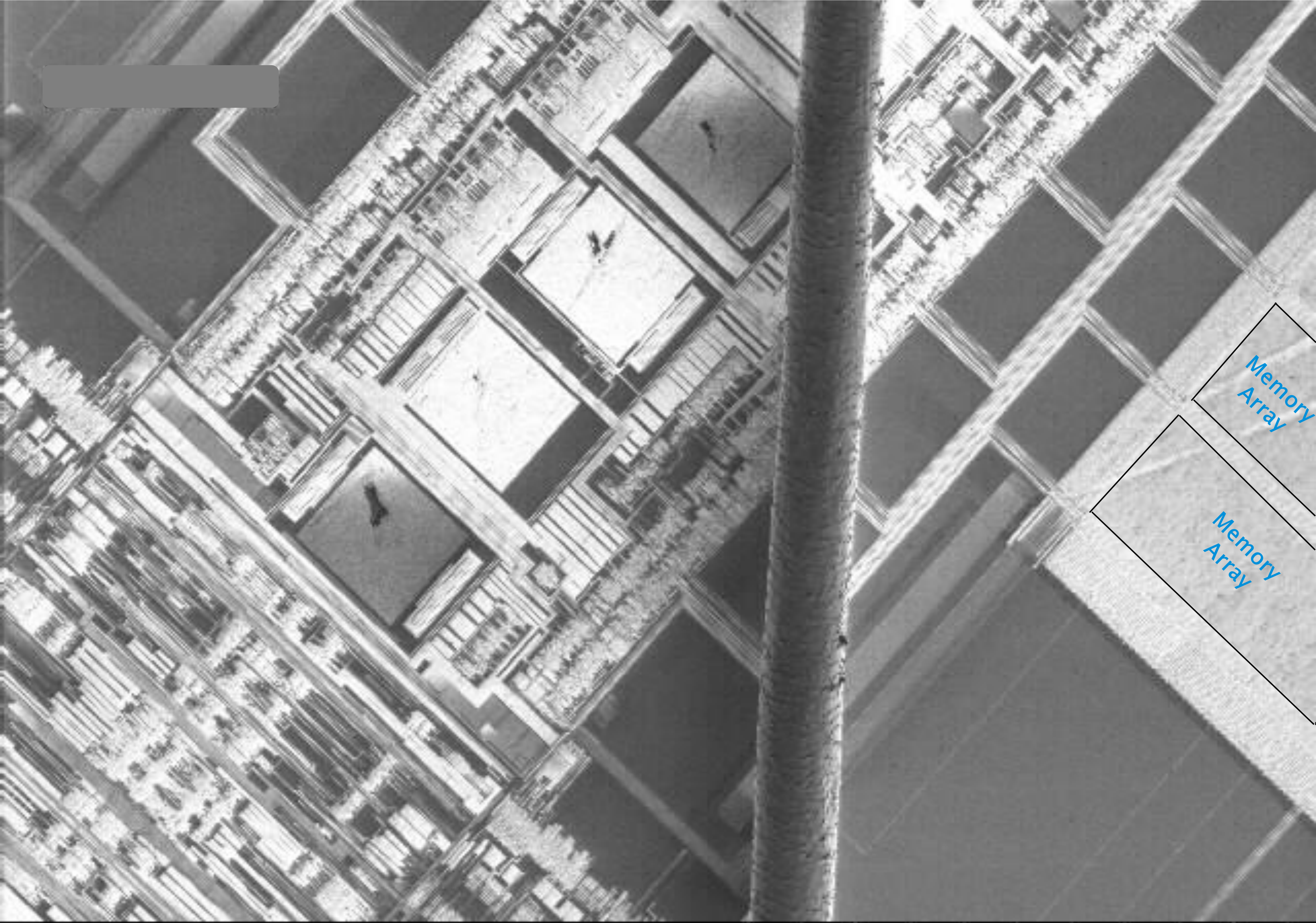
NITRIDE DEPOSIT [DIFFUSION]

- In the **Diffusion Area** a thin film of silicon nitride is deposited on top of the Pad Oxide. This film will be used later in the flow as a stop layer for a polishing process.
- Silicon nitride is usually referred as “nitride”

Detail Close-up



Silicon Nitride
Silicon Substrate



Circuit Elements with Human Hair

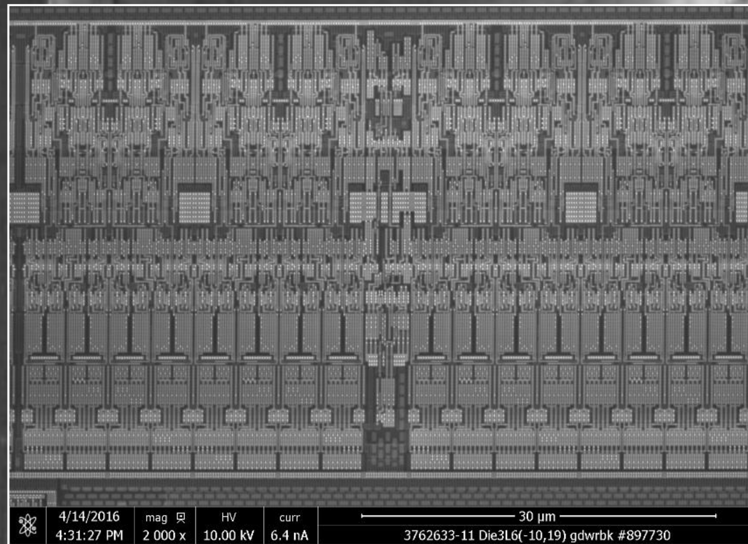
This hair is ~60 μ wide.

Hair may range 40-120 μ wide.

Circuit Elements with Human Hair

Circuit Elements with Human Hair

~60um

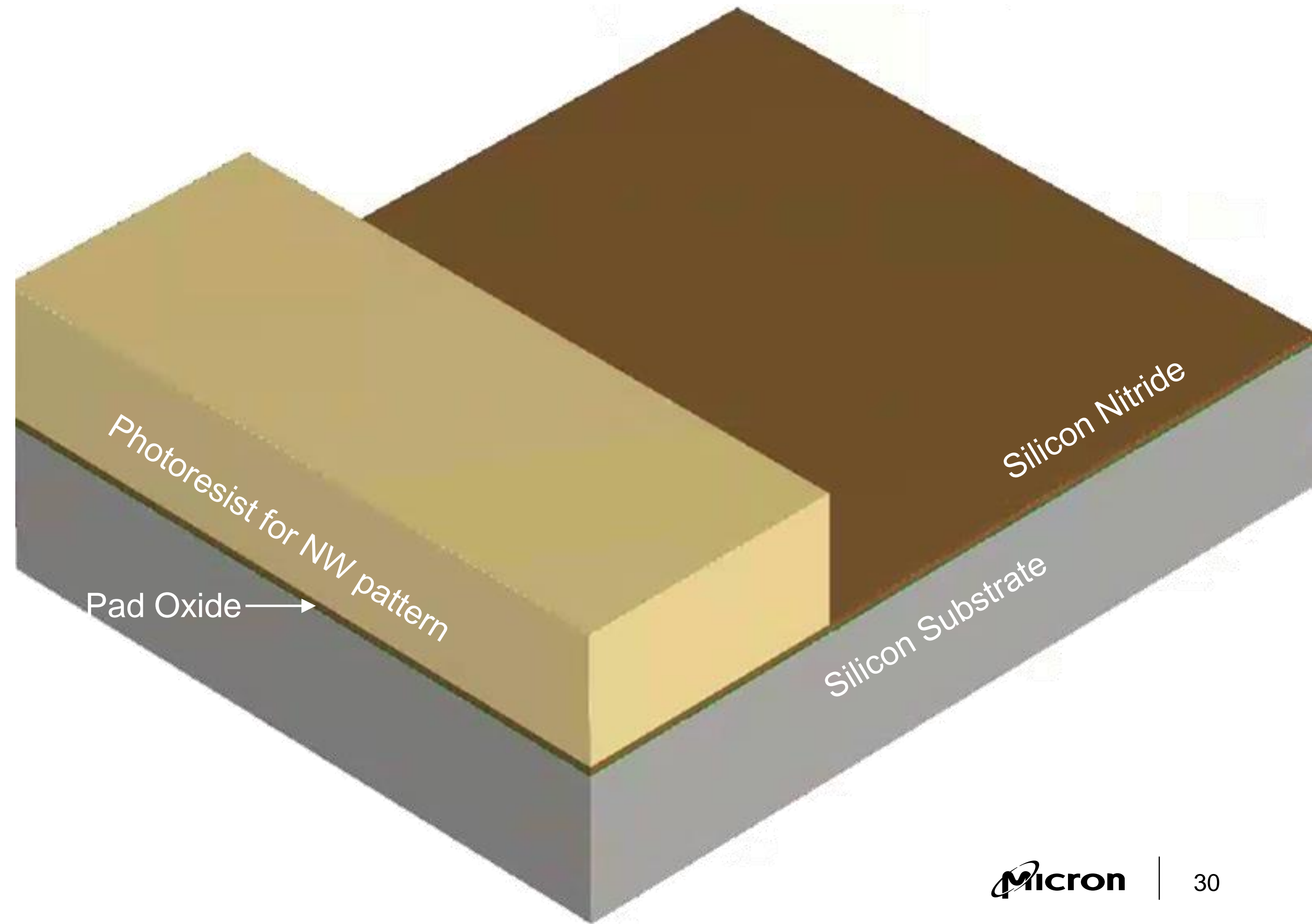


S4800 1.0kV x800 SE(M) 3/4/2004 16:26

50.0um

NW N-WELL PHOTO PATTERN [PHOTO]

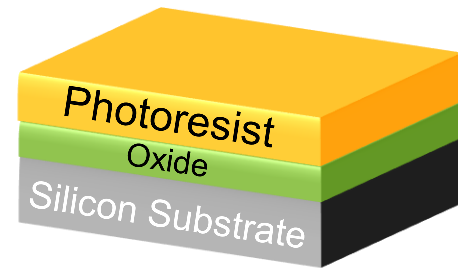
- In the **Photolithography Area** the “NW” reticle or mask is used to define a pattern in photoresist. The pattern will open certain areas where N-Wells are needed for the formation of PMOS transistor devices.
- Metrology:
  - Resist Thickness: ~ very thick to block implant



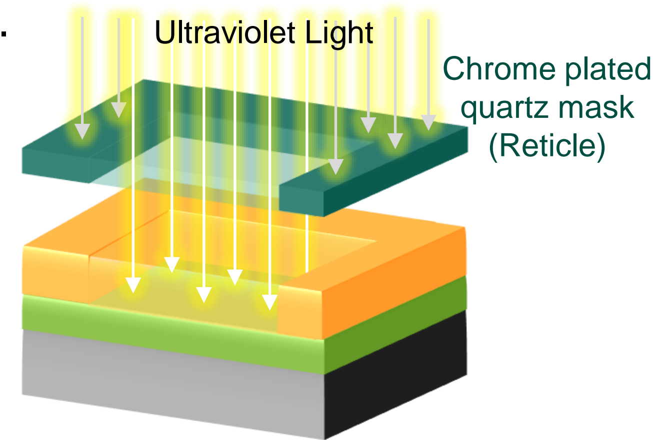
Photolithography

- The Photolithography area defines a temporary pattern that other areas (usually Dry Etch or Implant) use as a mask to create the structures needed on the wafer.
- The temporary pattern is created on a photosensitive film called photoresist (or resist).
- Patterns created on the wafer follow the five steps shown below.

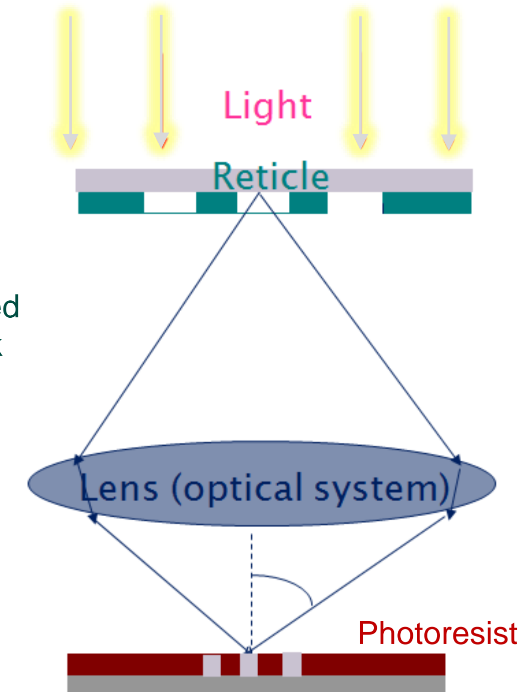
- The first three of these steps are performed in the photo-lithography area
- Immersion 193nm can print features down to 37nm and EUV can achieve ~15nm
- Modern Travelers have several dozen patterning levels
- Photoresist is “sacrificial” since it is only used temporarily to define patterns and once used any remaining film is removed.

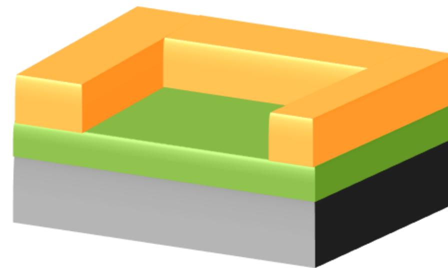


1. Apply Photoresist

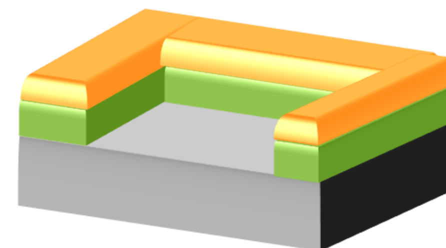


2. Expose Photoresist

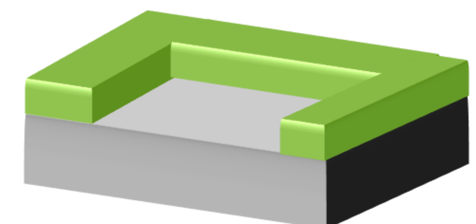




3. Develop (remove exposed photoresist)



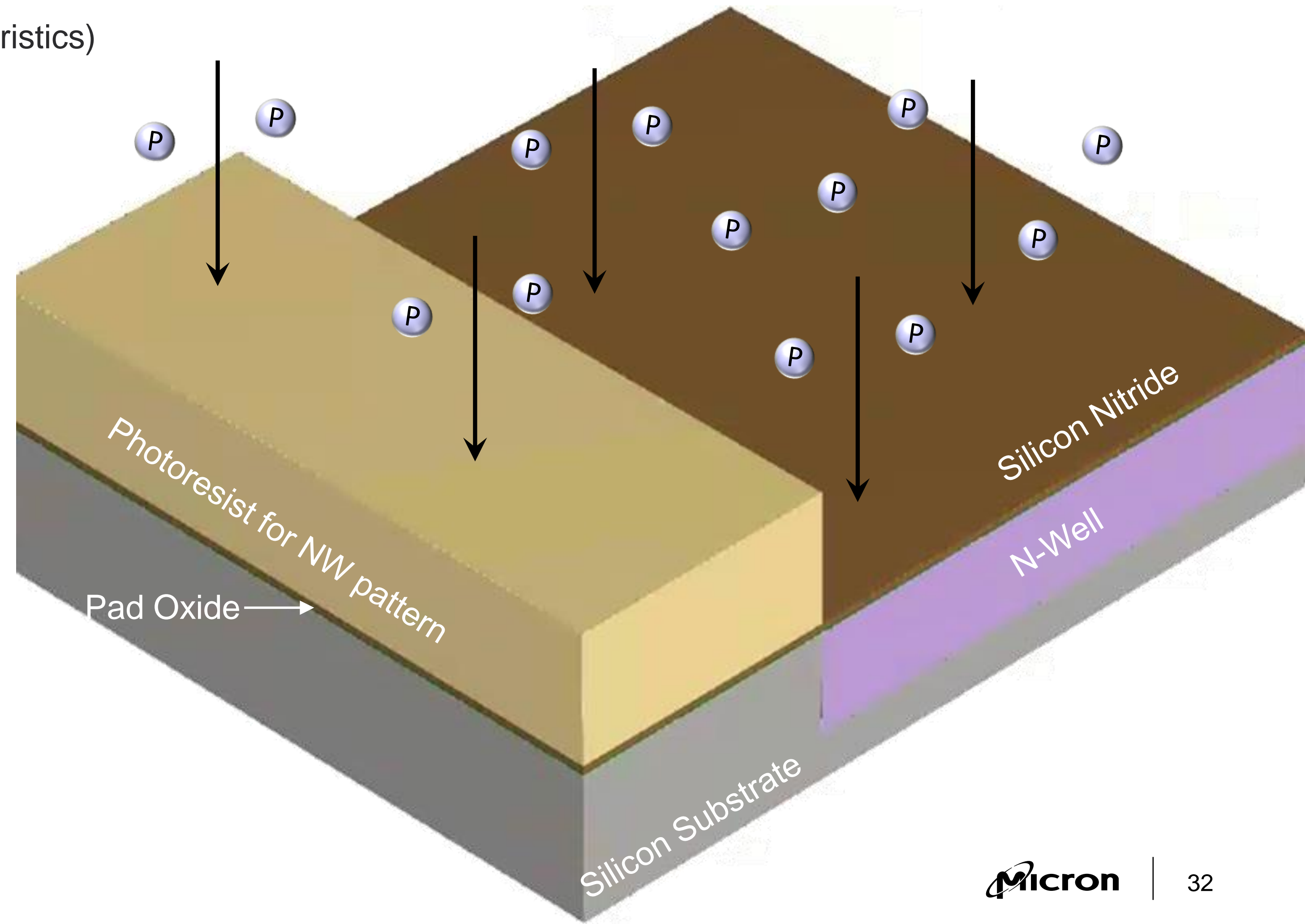
4. Etch (or Implant)



5. Strip Photoresist

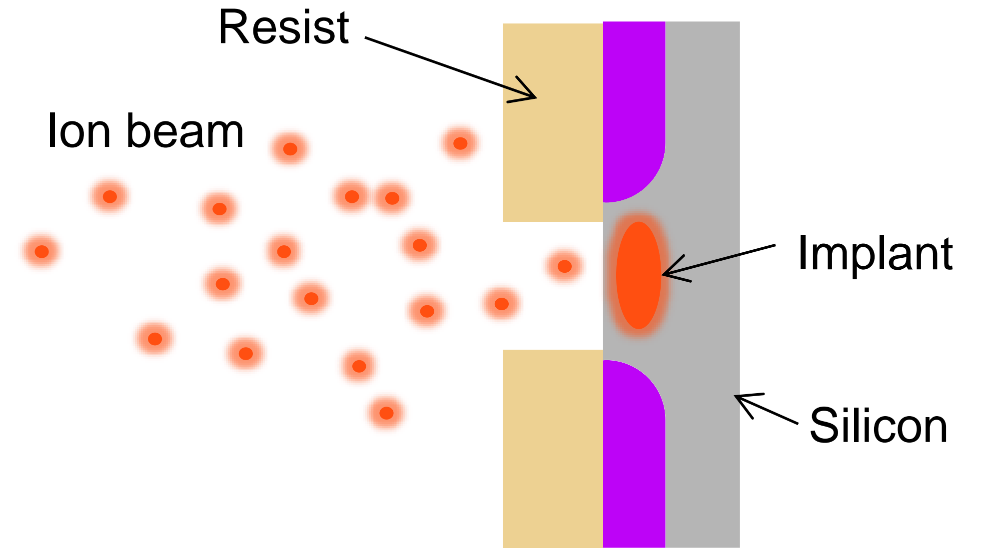
NW N-WELL IMPLANT [IMPLANT]

- In the **Implant Area** an ion implanter shoots phosphorous ions deep into the silicon to create an N-Well. The N-Well will provide the background doping needed to form PMOS transistors. The thick photoresist prevents the ions from entering the wafer in areas where N-Wells are not needed.
- Metrology:
  - Implant Depth: deep implant
  - Implant Dose: Low (needed for transistor characteristics)



Ion Implantation

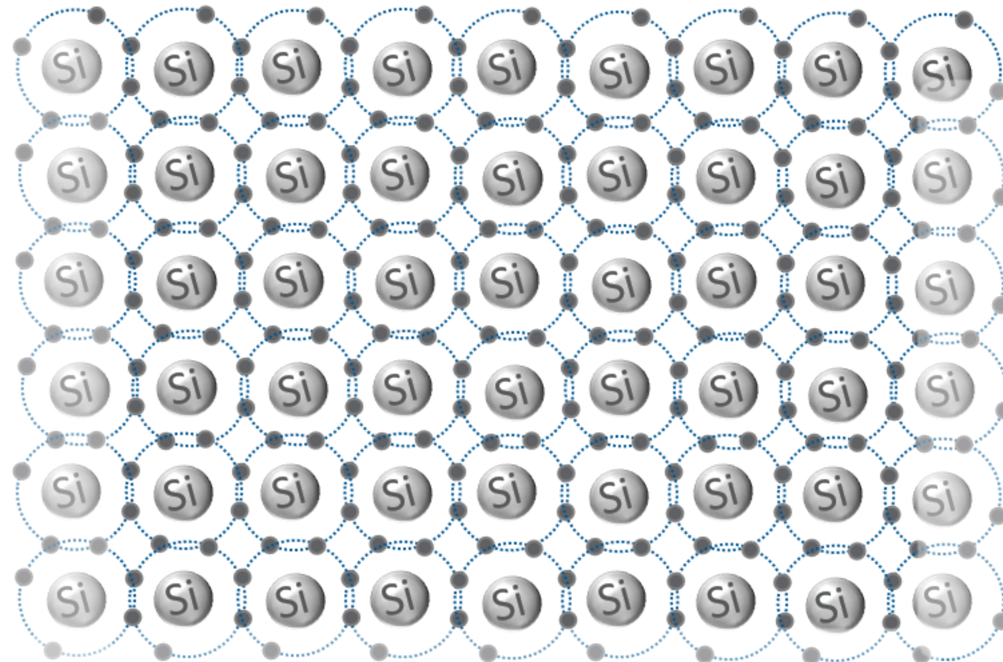
- Dopants are introduced into the silicon via a high-energy beam of ions that is directed at the wafer surface.
- The electrical properties of the silicon wafer are modified by “doping” with selected impurities.
- The most common dopants are boron, phosphorous, and arsenic.
- In most cases, a photo pattern using thick resist is used to prevent the dopants from entering unwanted areas of silicon.



Picture of preventive maintenance work on an Implant tool

Ion Implantation & Heat Treatment

- After all dopants are introduced/implanted, wafers are generally run through a high temperature heat treatment to **anneal** initial CMOS implants



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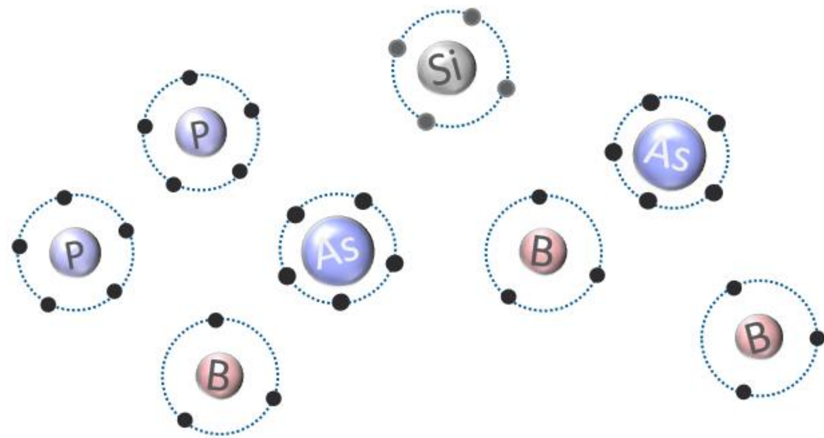
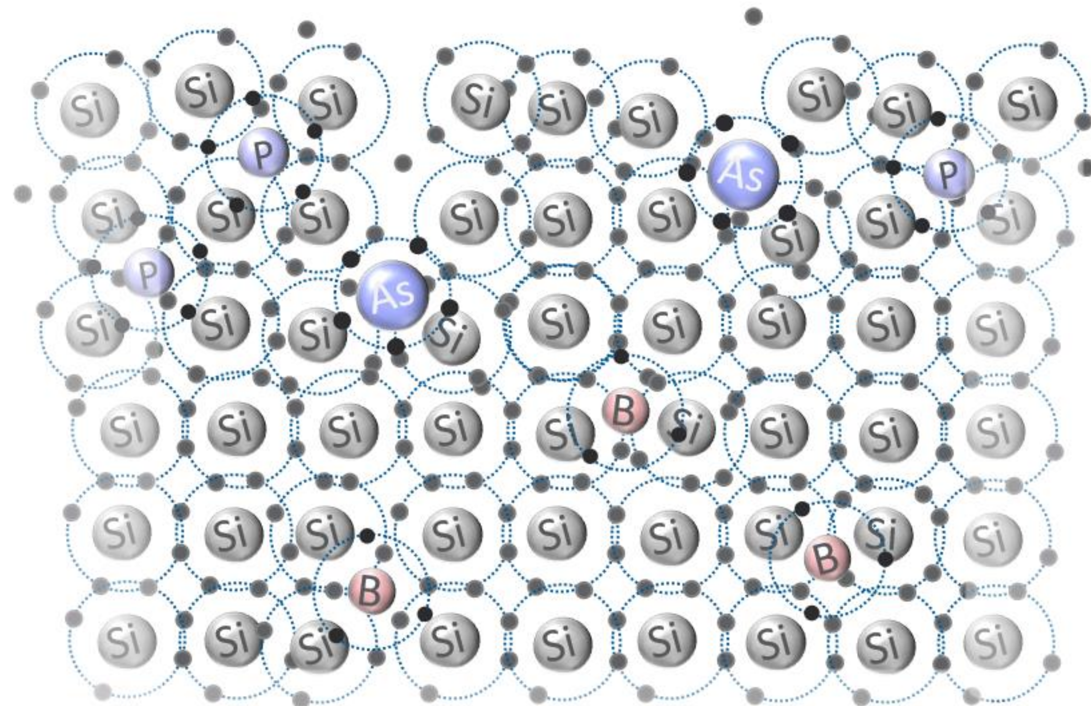


Before Anneal



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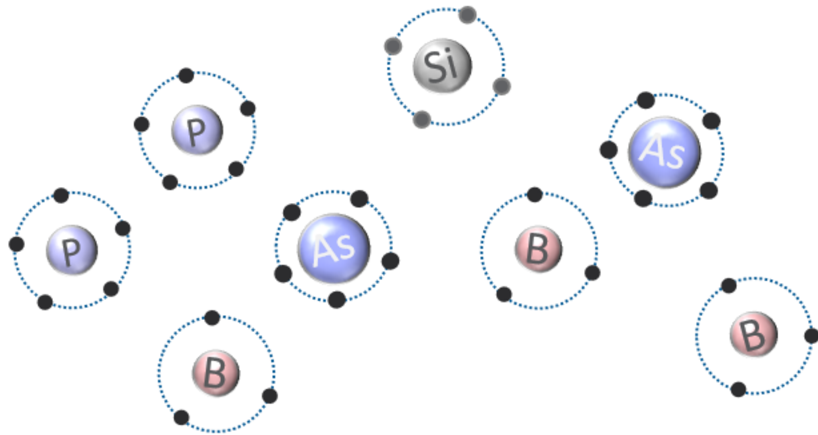
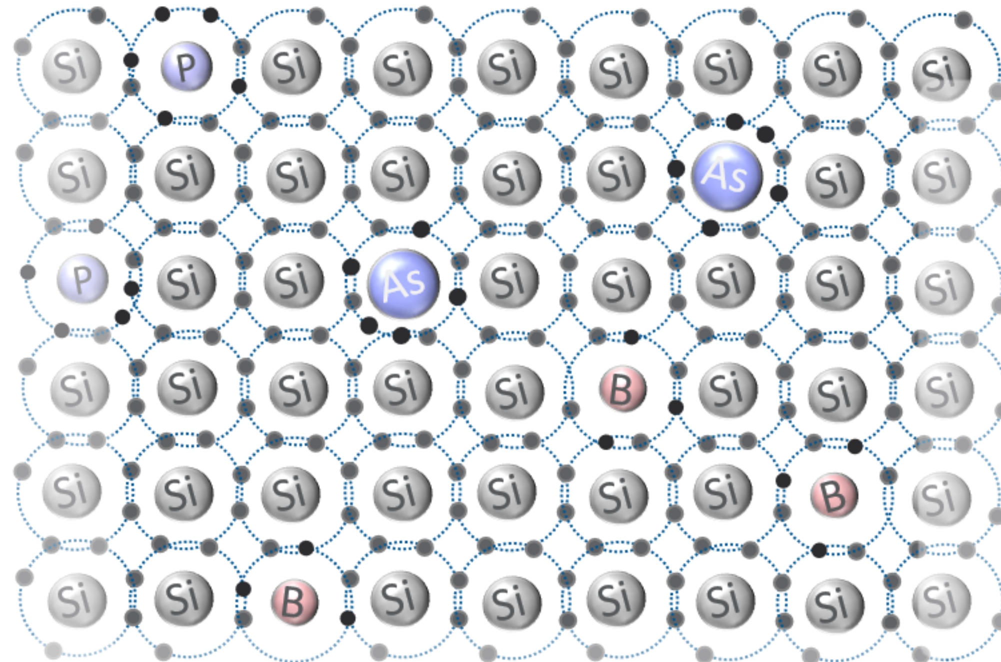
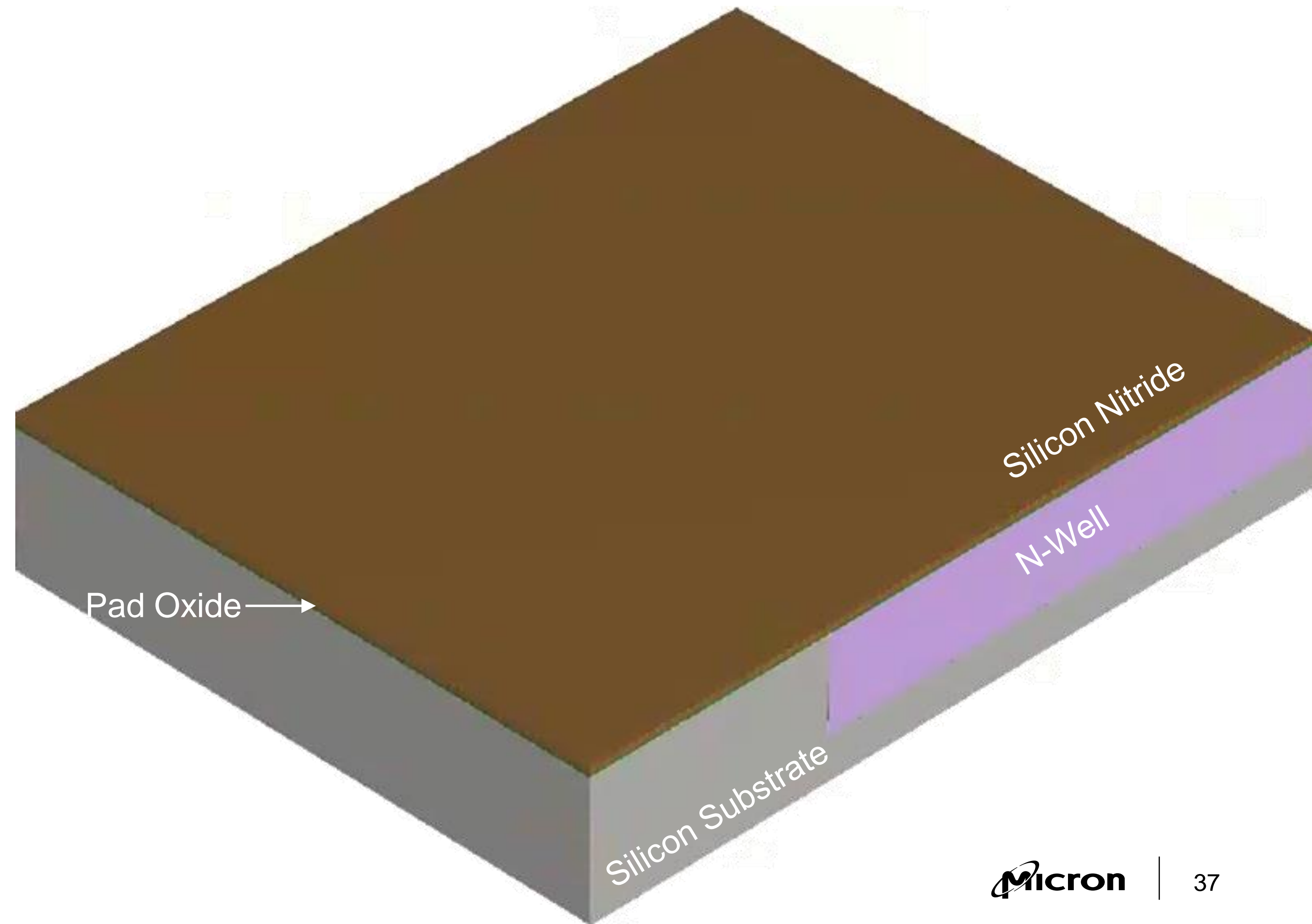


After Anneal

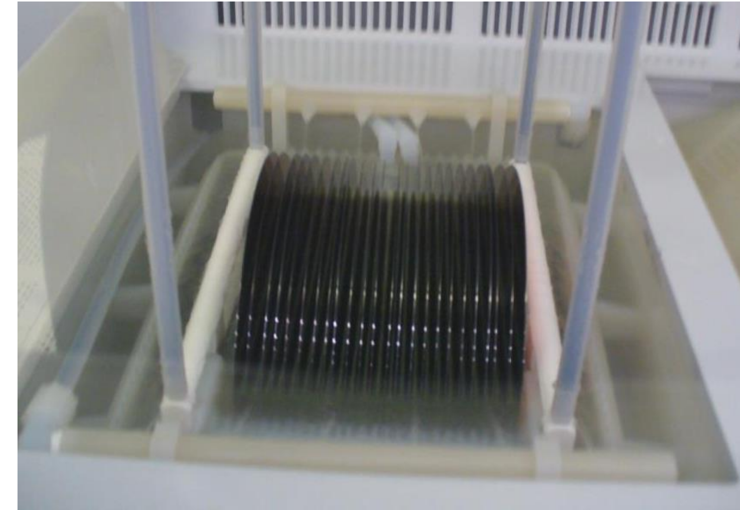


NW RESIST STRIP [WET PROCESS]

- In the **Wet Process Area** plasma and wet chemistry are used to remove the photoresist after the implant is complete.
- Metrology:
  - There should be no residual resist left on the wafer.



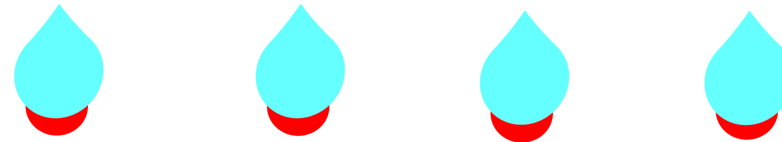
Wet Process – Wafer Cleaning



- The Wet Etch area uses chemical baths and de-ionized water to remove films and clean wafers to reduce defectivity.
- After every patterning operation, one or more wet process steps are used to remove the leftover photoresist and clean up residual organics, particles, and other forms of contamination.
- Wet process steps make up the largest percentage of the traveler.
- Multiple different chemistries are used to “selectively” remove some materials while leaving critical layers untouched.

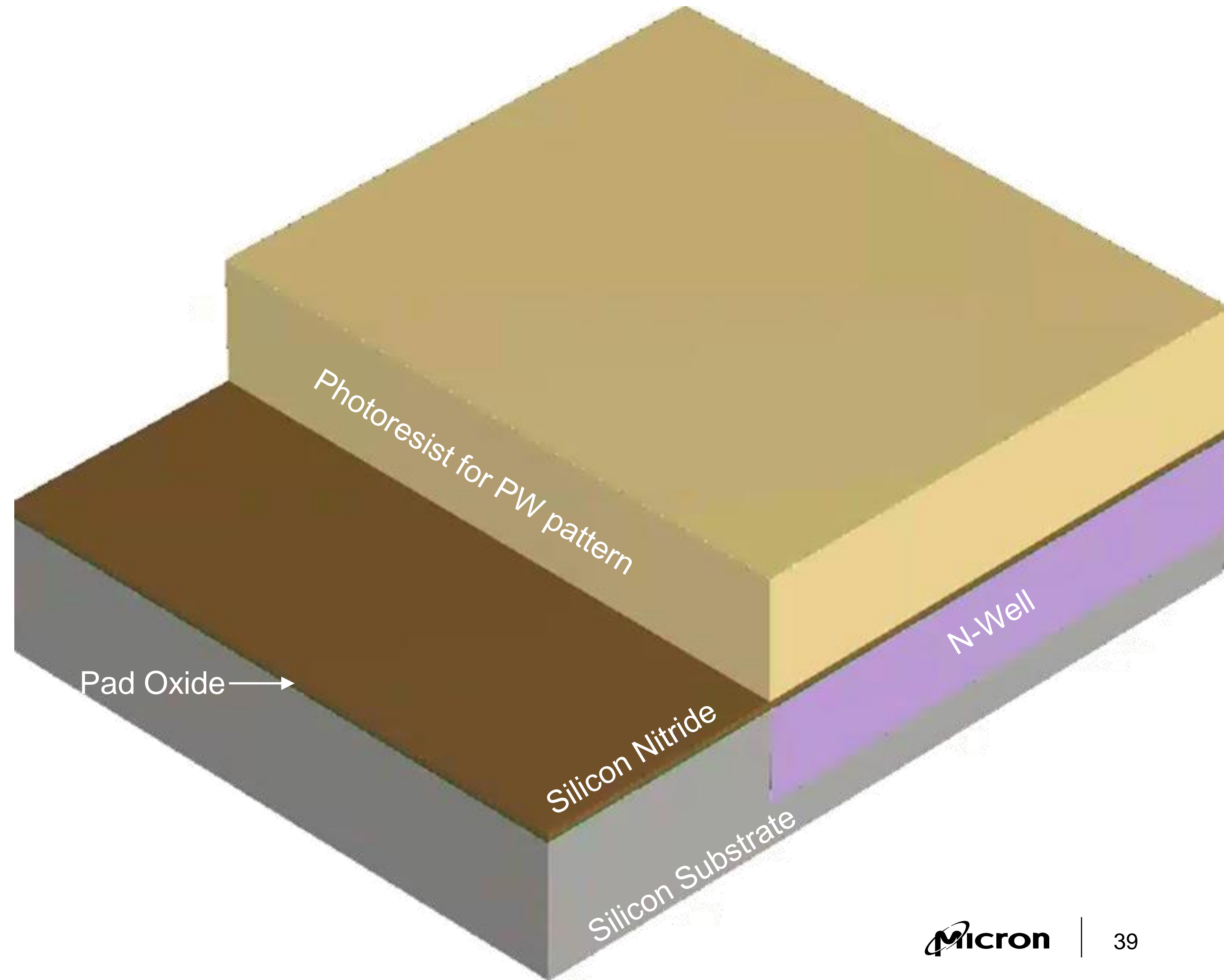
Typical Wet Etch Process:

1. Wafer is immersed in or sprayed with wet chemicals
2. Wet chemicals react with solid film constituents to break them down into solution
3. Wafer is immersed in or sprayed with DI water
4. DI water rinses away residual by-products and chemicals



PW P-WELL PHOTO PATTERN [PHOTO]

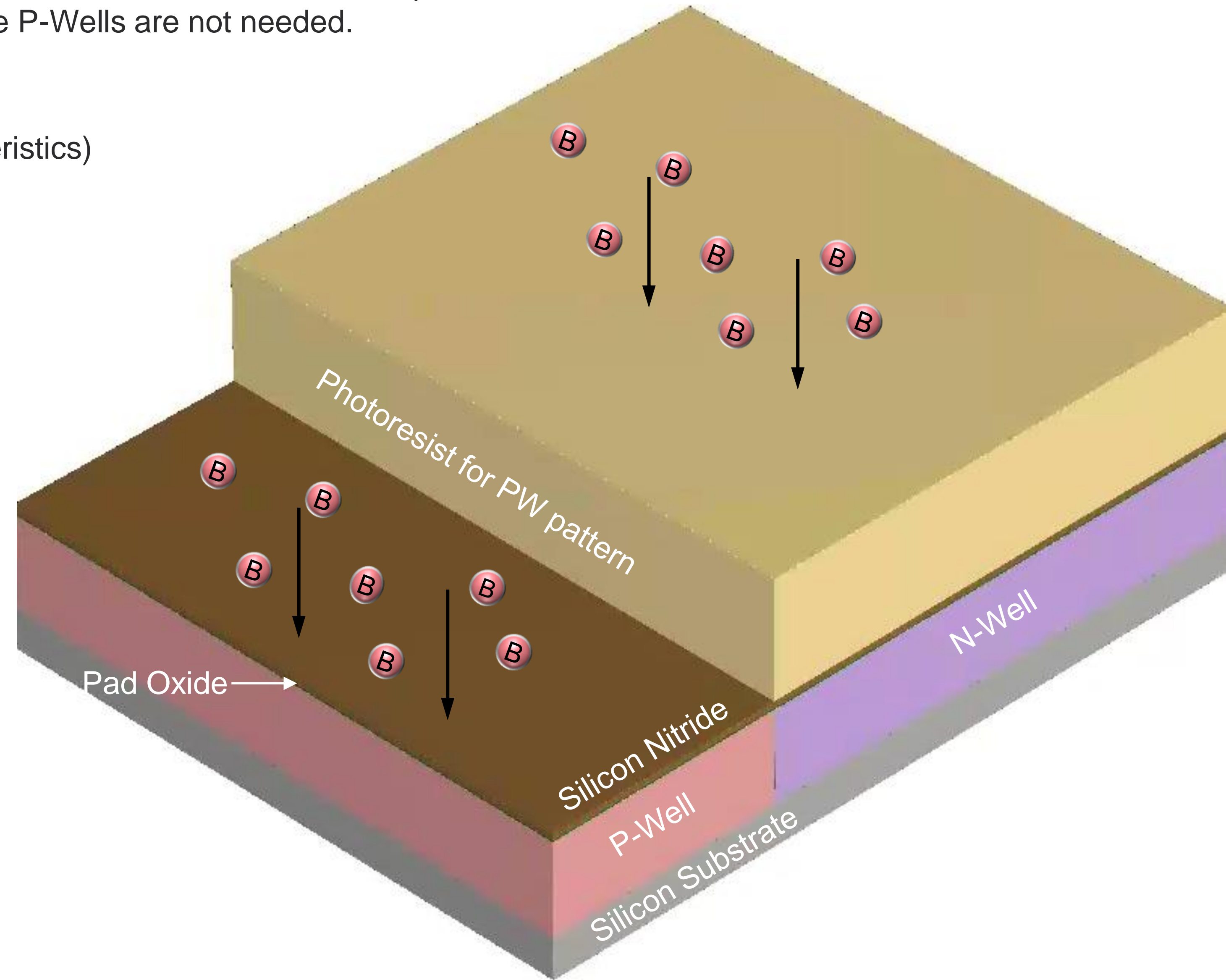
- In the **Photolithography Area** the “PW” mask is used to define a pattern in photoresist. The pattern will open certain areas where P-Wells are needed for the formation of NMOS devices.
- Metrology:
  - Resist Thickness: very thick to block implant



PW P-WELL IMPLANT [IMPLANT]

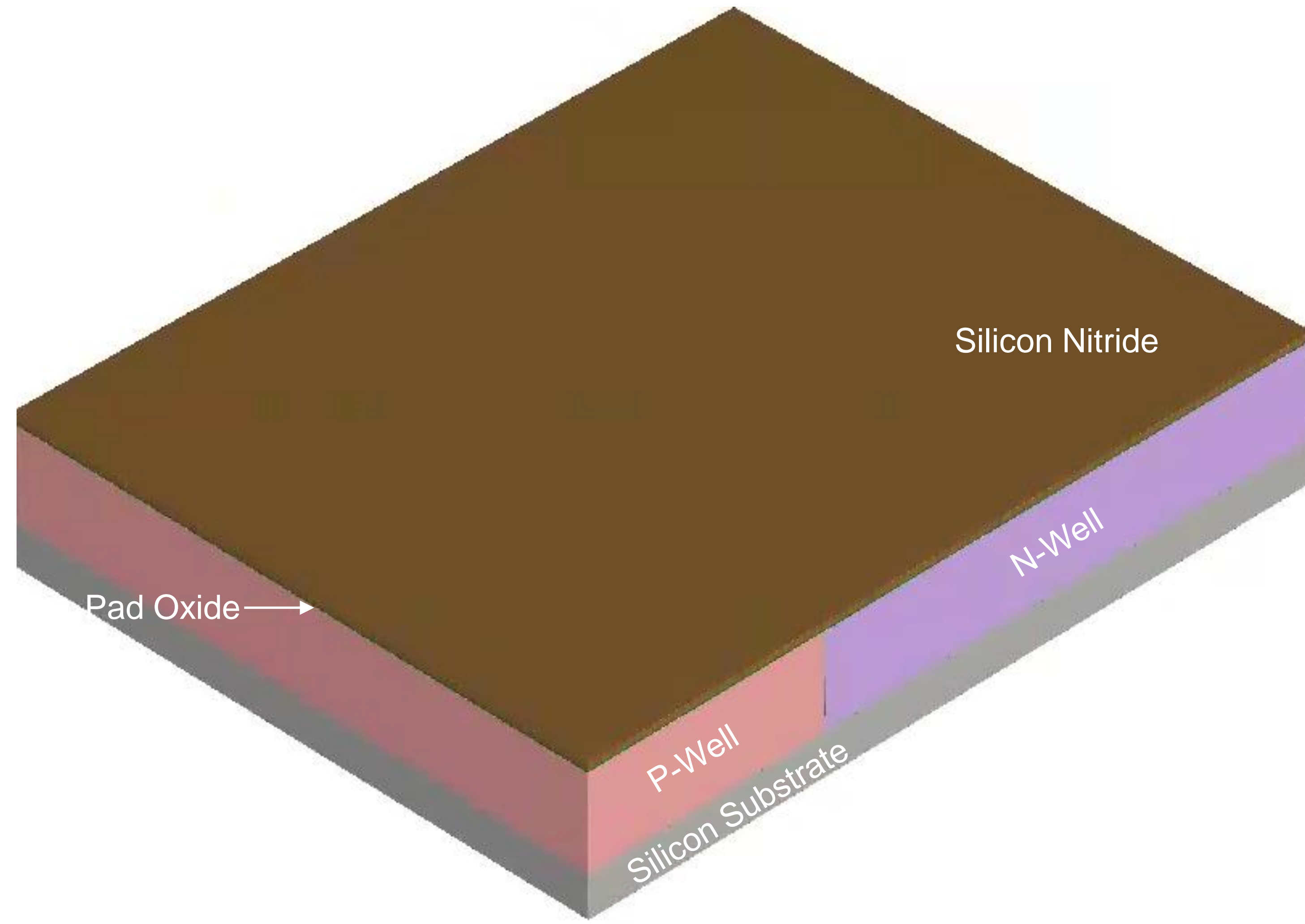
- In the **Implant Area** an ion implanter shoots boron ions deep into the silicon to create a P-Well. The P-Well will provide the background doping needed to form NMOS transistors. The thick photoresist prevents the ions from entering the wafer in areas where P-Wells are not needed.
- Metrology:
  - Implant Depth: deep implant
  - Implant Dose: Low (needed for transistor characteristics)

Q) What do you think is the next Traveler step?



PW RESIST STRIP [WET PROCESS]

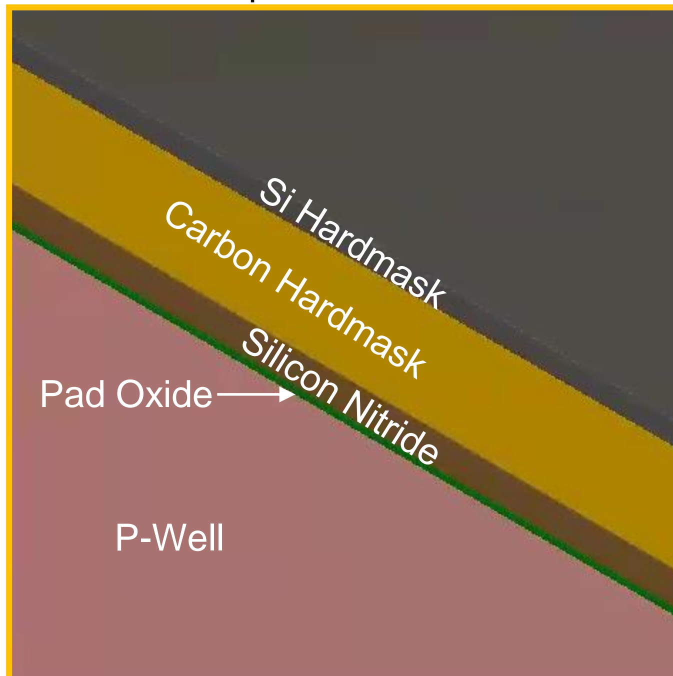
- In the **Wet Process Area** plasma and wet chemistry are used to remove the photoresist after the implant is complete.
- Metrology:
  - There should be no residual resist left on the wafer.



AA HARDMASK LAYERS DEPOSIT
[CHEMICAL VAPOR DEPOSITION (CVD)]

- In the **CVD Area** a thick film of carbon (C) is deposited followed by a thin silicon-based (Si) film. Together these films comprise a “hardmask” which allows us to etch very small features while keeping the photoresist layer as thin as possible. Hardmasks are prevalent throughout this CMOS flow.

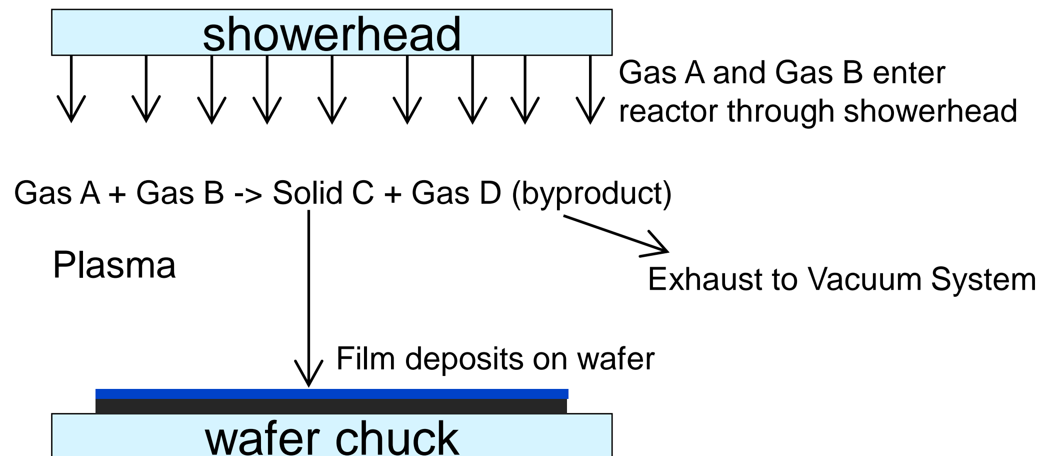
Detail Close-up



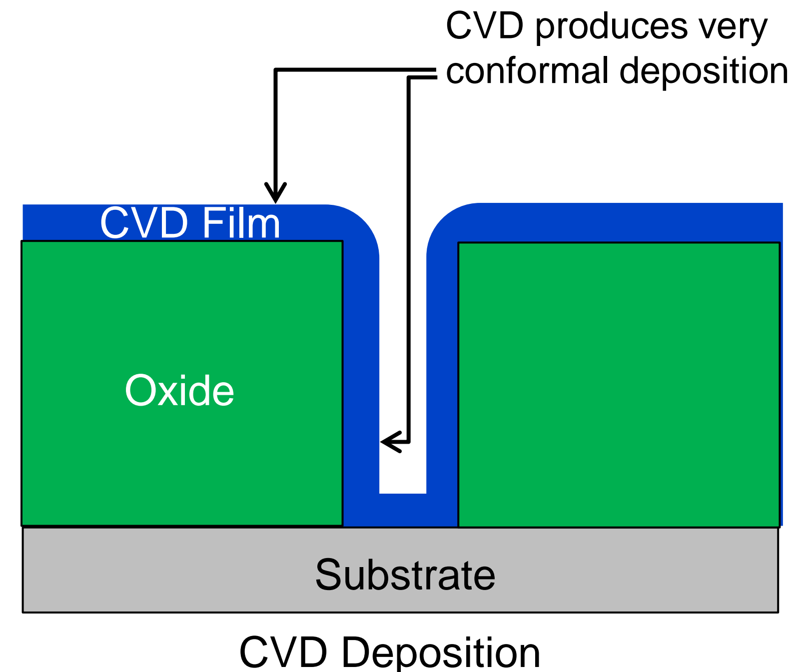
Si HM
C HM
N-Well
P-Well
Silicon Substrate

Chemical Vapor Deposition (CVD)

- CVD is used to deposit a variety of insulating and conductive films at multiple places in the Traveler.
- Gases are introduced into a chamber. A solid film, which is a product of the reaction, deposits on the wafer.
- Most CVD processes also use plasma technology (similar to dry etch).
- Compared to other deposition methods, CVD films can be very conformal, allowing us to fill very narrow holes and trenches without creating voids or gaps.



CVD Reactor – Vacuum Chamber



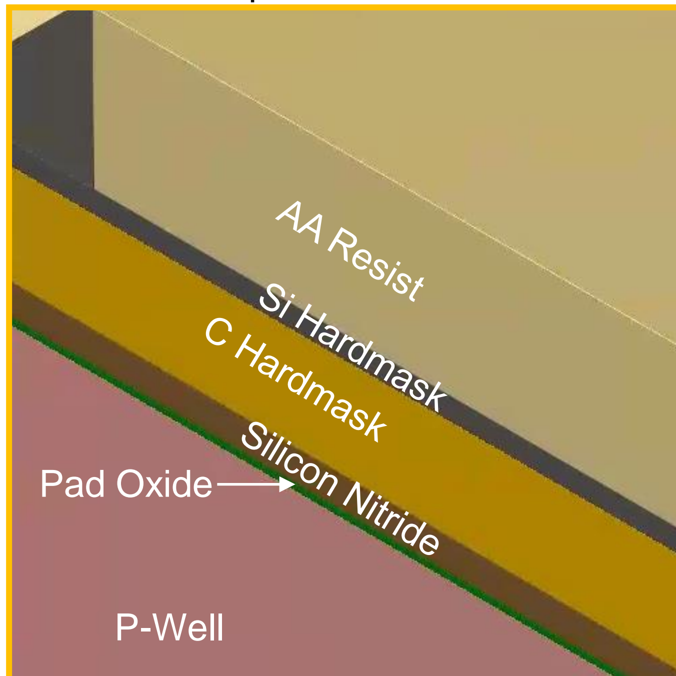
CVD Deposition

[Compare with PVD]

AA ACTIVE AREAS PHOTO PATTERN [PHOTO]

- In the **Photolithography Area** the “AA” mask is used to define a pattern in photoresist. The pattern defines “active areas” where CMOS devices will be formed. Between the active areas, trenches will be etched into the silicon substrate to provide electrical isolation between devices.

Detail Close-up

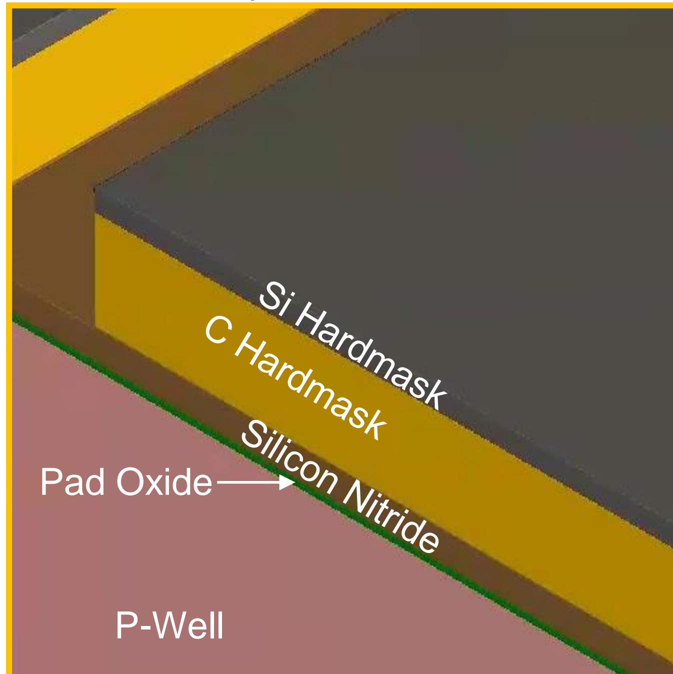


AA Resist
Si HM
C HM
N-Well
P-Well
Silicon Substrate

AA HARDMASK DRY ETCH [DRY ETCH]

- In the **Dry Etch Area** a plasma process is used to transfer the AA photoresist pattern into the underlying hardmask layers. The hardmask layers will provide a more robust mask for the subsequent trench etch than photoresist.
- Notes:
  - This step is also known as “Dry Develop”
  - The photoresist is completely etched away in this step.

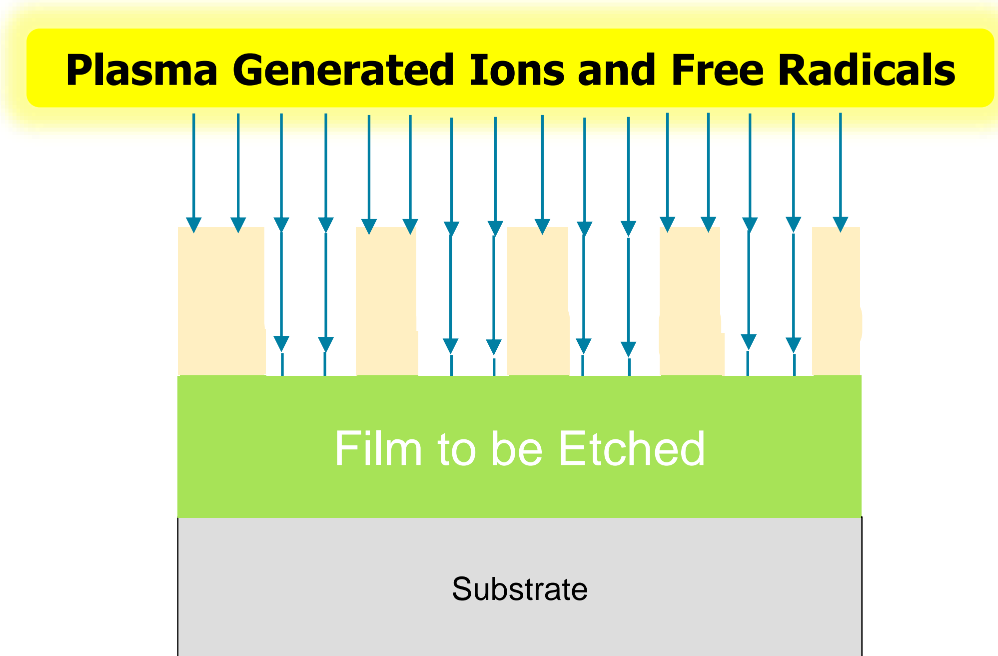
Detail Close-up

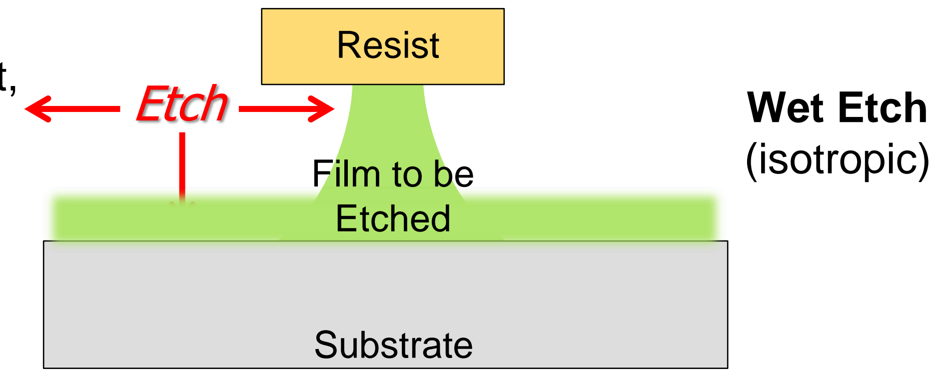


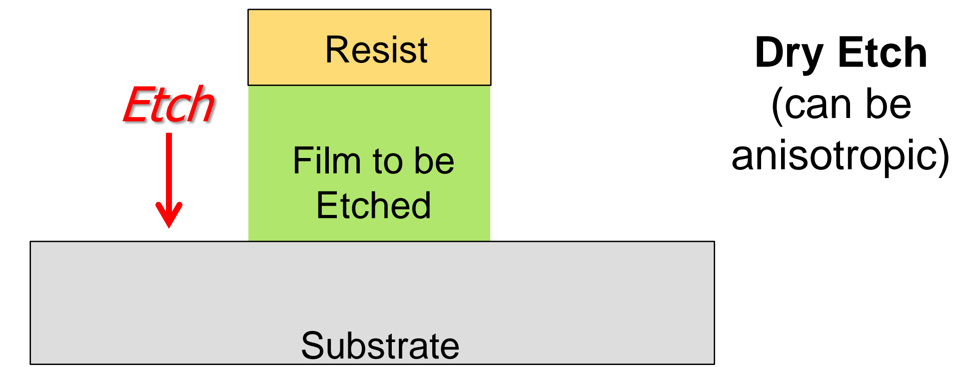
Si HM
C HM
N-Well
P-Well
Silicon Substrate

Dry Etching

- The Dry Etch area **removes** (etches) films using plasma (ionized gases). Dry Etch usually processes wafers after a temporary mask has been previously patterned, e.g. photoresist or a hardmask. The mask protects some regions of the wafer. Dry Etch only removes films from the unprotected regions. Very fine and precise patterns can be etched into films.
- Dry etch utilizes plasma technology to permanently transfer a mask pattern into the underlying layer(s).
- Wet processing can also be used for patterning, but wet process is isotropic while dry etching can be vertical (anisotropic). Dry Etch allows for much more accurate and precise feature definition.
- Dry etch can further reduce dimensions through sidewall etching or undercut, resulting in a smaller feature than what only Photo can produce (< 20 nm).





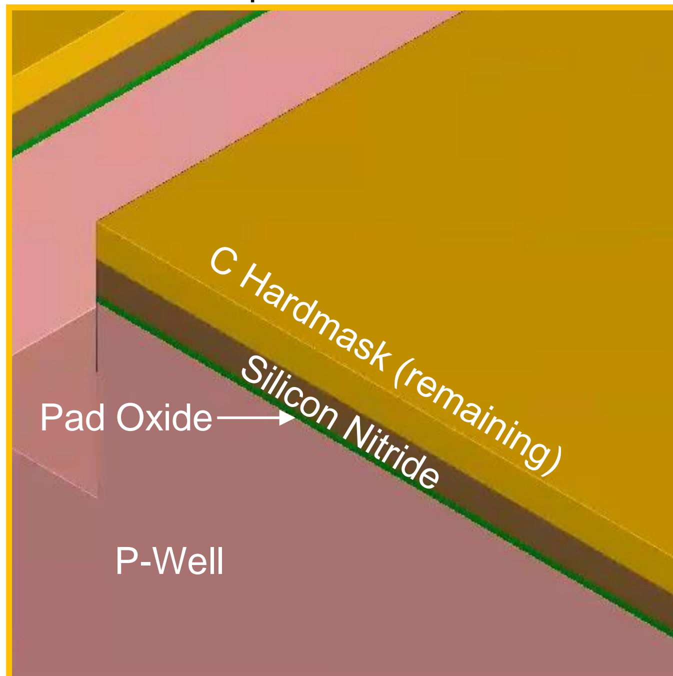


AA STI DRY ETCH [DRY ETCH]

- In the **Dry Etch Area** a second plasma process is used to etch trenches into the silicon wafer. For this process the mask is the Si hardmask and the carbon hardmask. These trenches will be filled with oxide and will provide electrical isolation between adjacent active areas.
- Notes:
  - STI stands for “Shallow Trench Isolation”
  - Some of the carbon hardmask layer remains after this etch is complete

Q) What do you think is the next Traveler step?

Detail Close-up



Carbon Hardmask (remaining)

N-Well

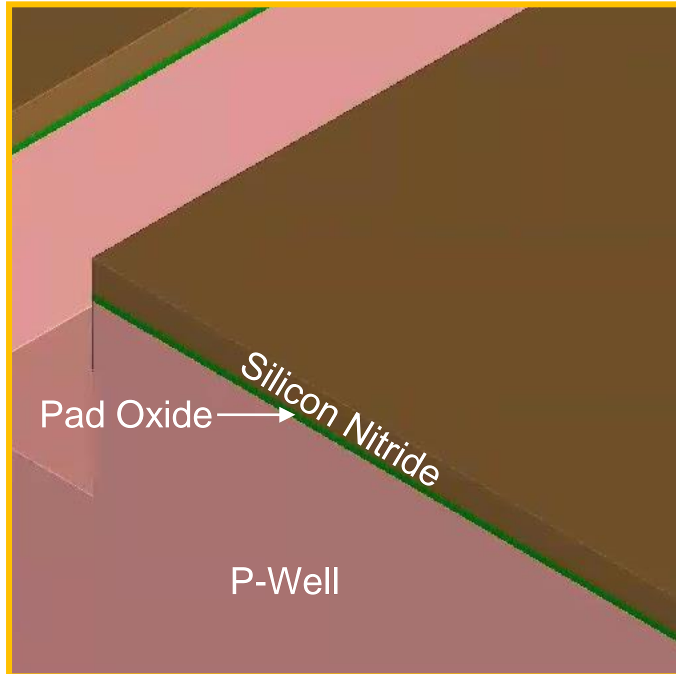
P-Well

Silicon Substrate

AA RESIST STRIP [WET PROCESS]

- In the **<u>Wet Process Area</u>** plasma and wet chemistry are used to remove the remaining carbon hardmask after the trench etch is complete (similar recipe used to remove photoresist)
- <u>Metrology:</u>
  - There should be no residual carbon left on the wafer.

Detail Close-up



Silicon Nitride

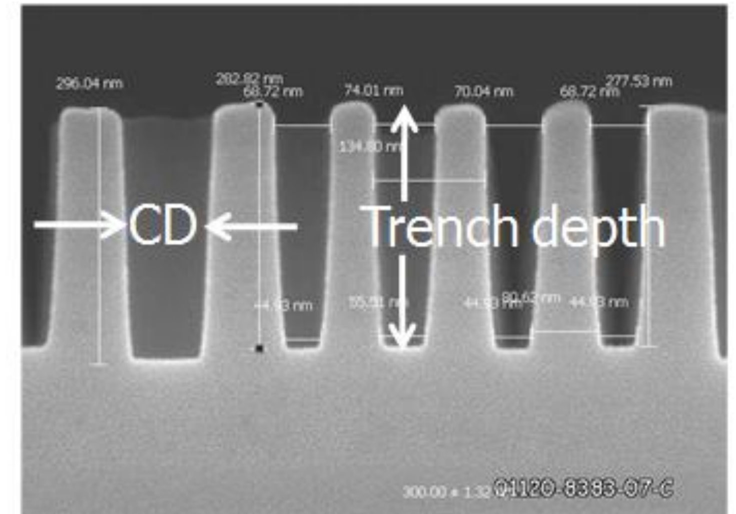
N-Well

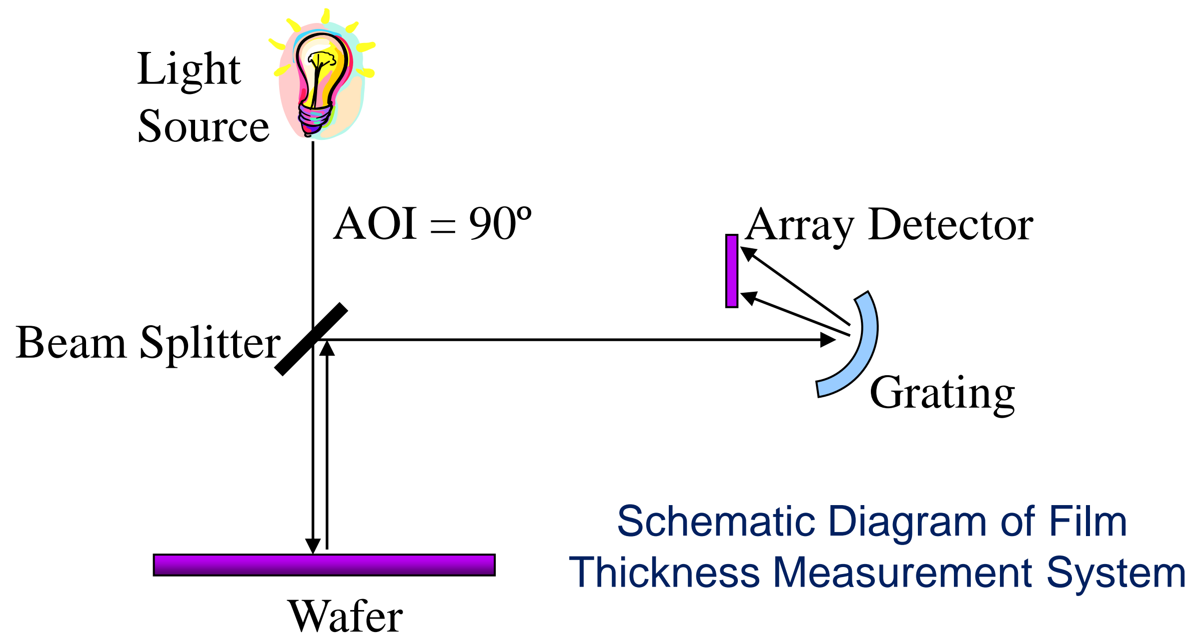
P-Well

Silicon Substrate

Metrology

- The Metrology area takes measurements that evaluate the results of process operations.
- Examples of measurements are film thicknesses, critical dimensions (CD's), lithography overlay, film resistivity, surface planarity, composition, and stress.
- At right is a cross section image of a wafer where several critical dimensions (CDs) were taken using a scanning electron microscope (SEM).
- Below is a schematic diagram of a system used to measure the thickness of very thin films. This technique uses the principle of optical interference.



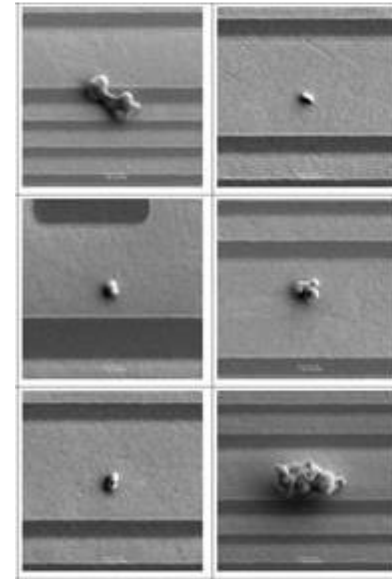


Schematic Diagram of Film Thickness Measurement System

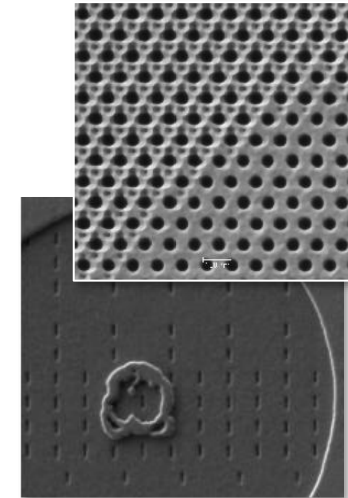
Real-Time Defect Analysis (RDA)

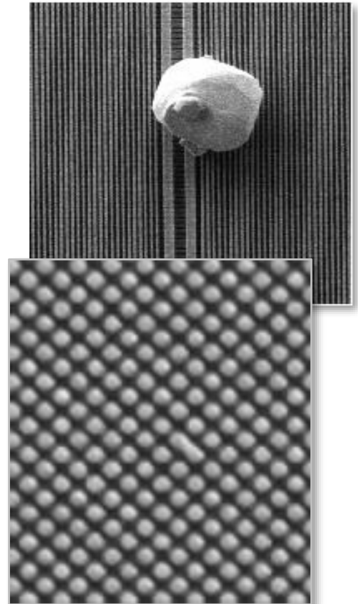
- The Real-Time Defect Analysis (RDA) area inspects wafers for defects at critical points in the manufacturing process.
- The RDA area monitors in-line wafers and provides critical data collection and analysis services to fab process areas
- The process areas use the information that RDA provides to reduce defectivity on the wafers

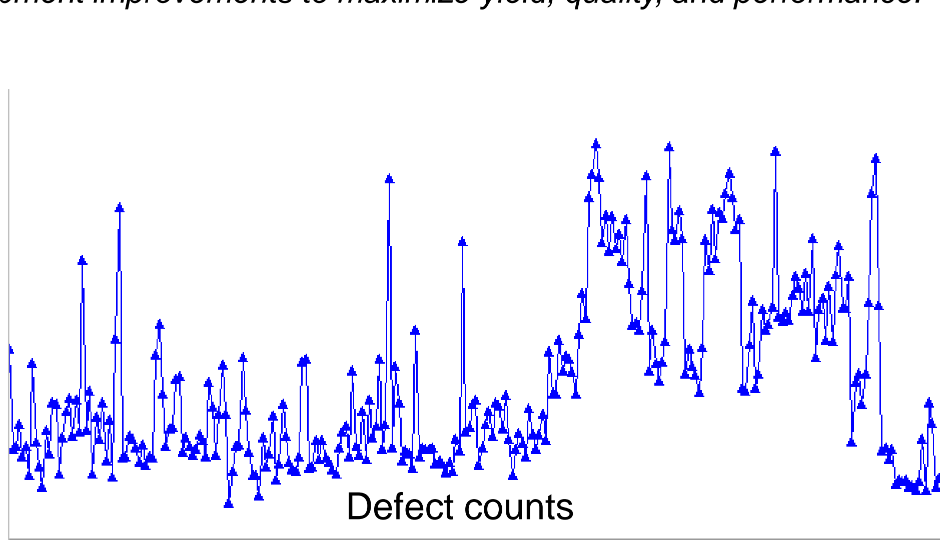
Metro & RDA do not alter the structural or electrical characteristics, however, for processing wafers from start to finish THEY ARE OUR EYES to what is happening on the wafers. THEY ARE CRITICAL for design, layout, reticle, process and equipment improvements to maximize yield, quality, and performance.



Physical defects

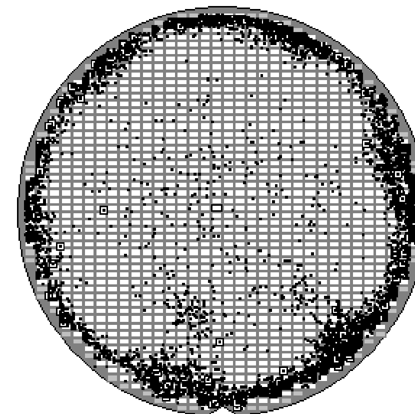






Defect counts

Defect Wafer Maps



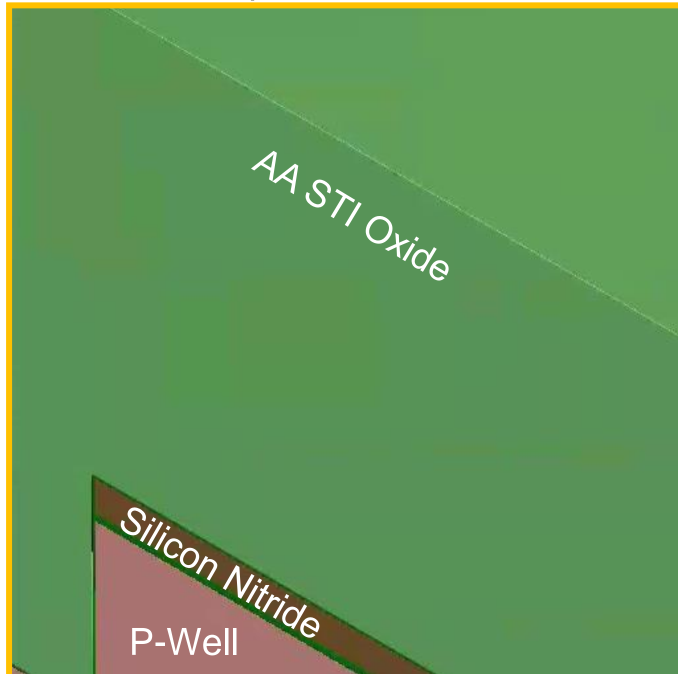
edge ring shading

AA STI OXIDE DEPOSIT [CVD]

- In the **CVD Area** a thick film of silicon dioxide is deposited to fill the trenches. Only the oxide in the trenches is needed, so the unwanted surface oxide will be removed in the next Traveler step.

Q) What do you think is the next Traveler step?

Detail Close-up

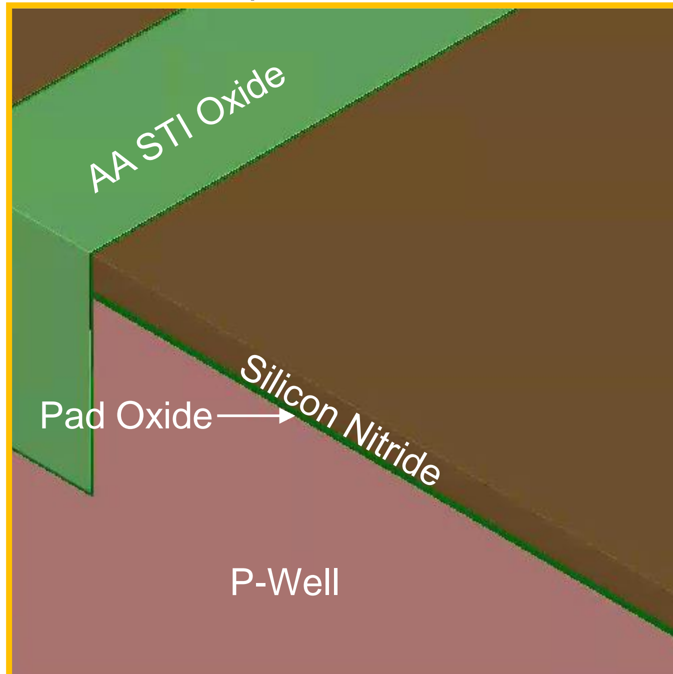


AA STI Oxide
N-Well
P-Well
Silicon Substrate

AA STI OXIDE CMP [CHEMICAL MECHANICAL PLANARIZATION]

- In the **CMP Area** a polishing process is used to remove the unwanted oxide on the surface, leaving the trenches filled with oxide.
- Note: The silicon nitride film, deposited near the beginning of the flow, effectively stops the CMP process. This process is referred to as a “Stop on Nitride (SON)” process.

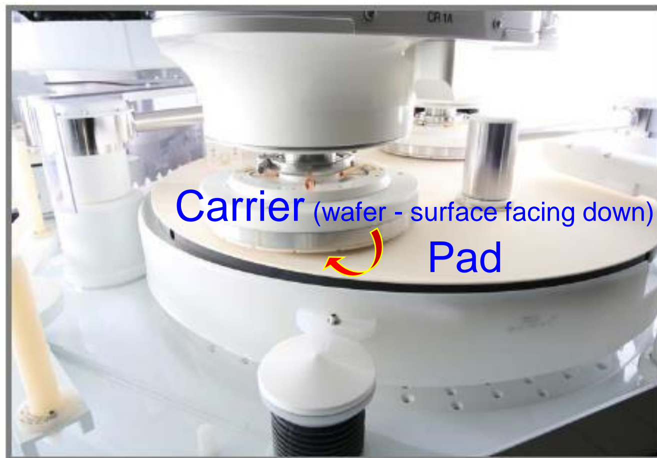
Detail Close-up



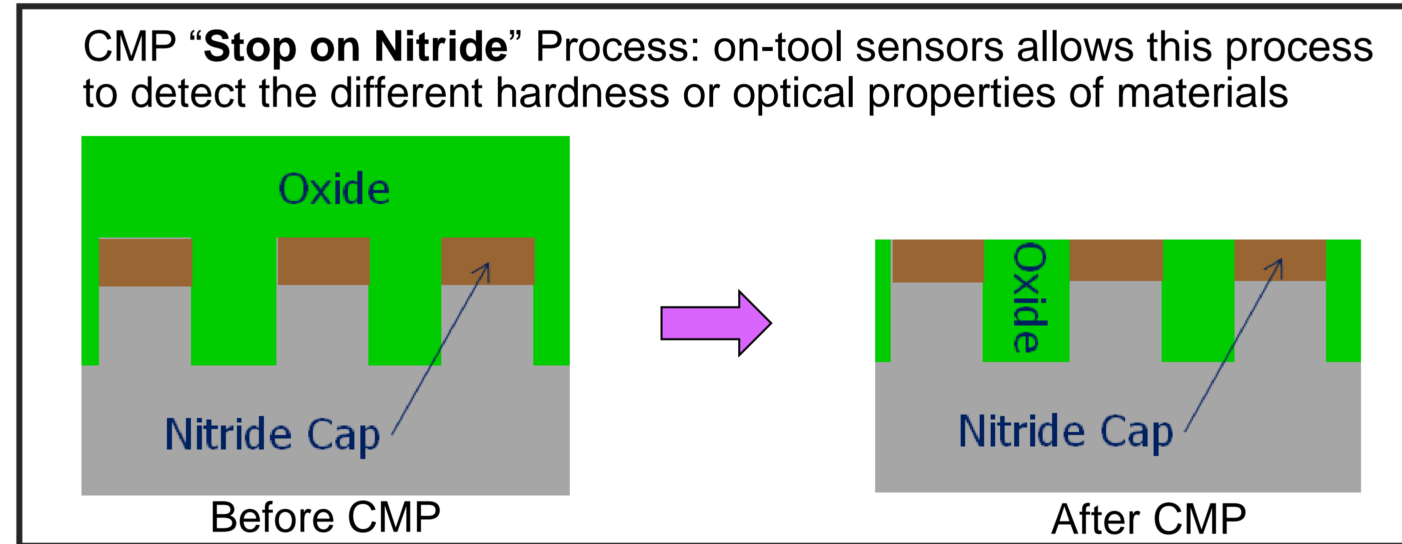
AA STI Oxide
Silicon Nitride
N-Well
P-Well
Silicon Substrate

Chemical Mechanical Planarization (CMP)

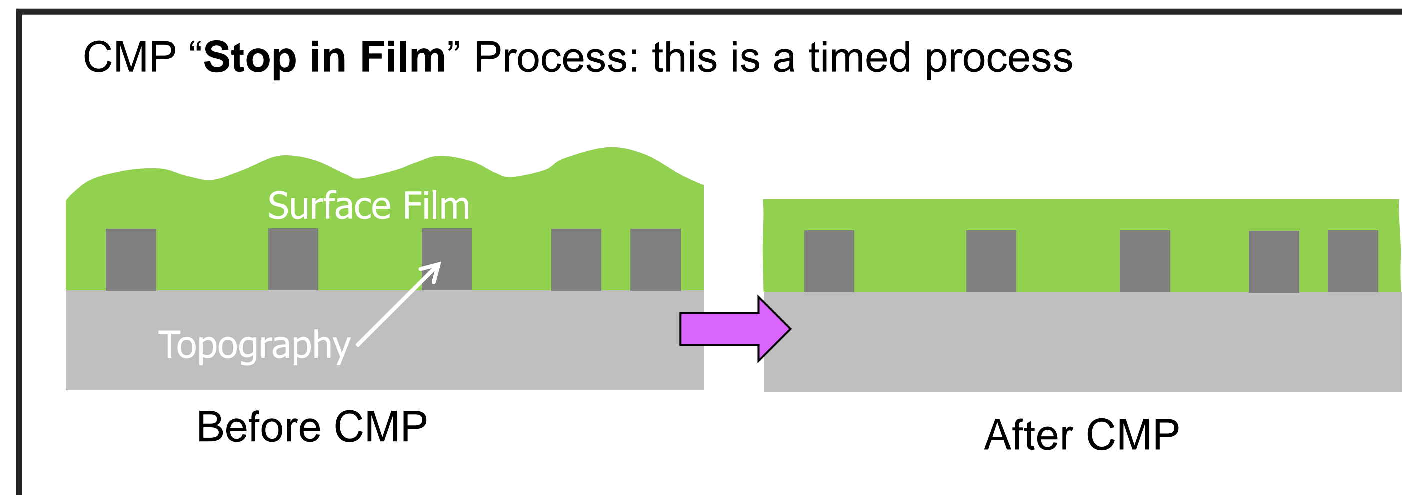
- CMP is used to reduce or eliminate topography on the wafer surface. A planar surface is necessary for photo to print patterns at very small feature sizes.
- CMP is also used to remove excess surface films after they have been deposited.
- CMP uses a polishing pad and a chemical slurry made of fine abrasive particles suspended in a dilute chemical solution to perform the polishing process.
- Like wet etch and dry etch, CMP can selectively polish some films while leaving others untouched.



CMP "**Stop on Nitride**" Process: on-tool sensors allows this process to detect the different hardness or optical properties of materials



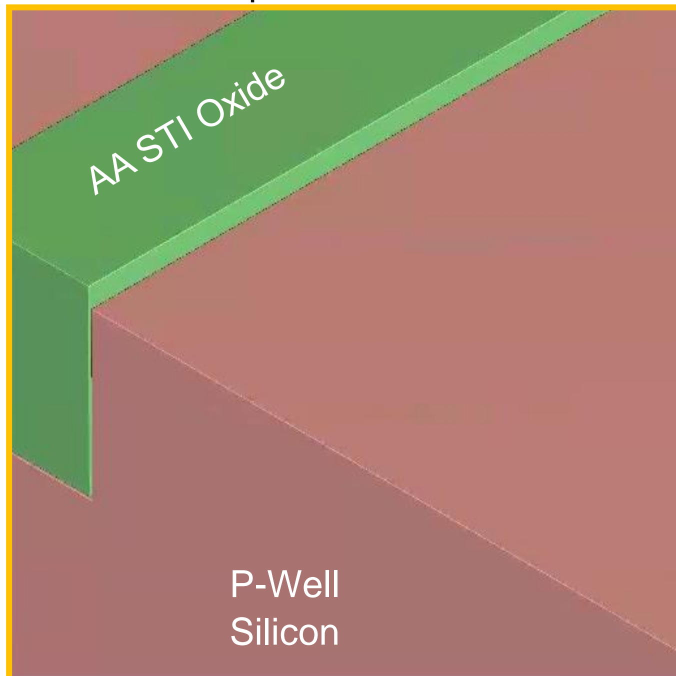
CMP "**Stop in Film**" Process: this is a timed process



AA STI NITRIDE WET ETCH [WET PROCESS]

- The nitride film is no longer needed, so in the **Wet Process Area** wet chemicals are used to completely remove the nitride with minimal impact to the exposed oxide or silicon layers.
- A second wet chemical process removes the original Pad Oxide, exposing bare silicon.

Detail Close-up

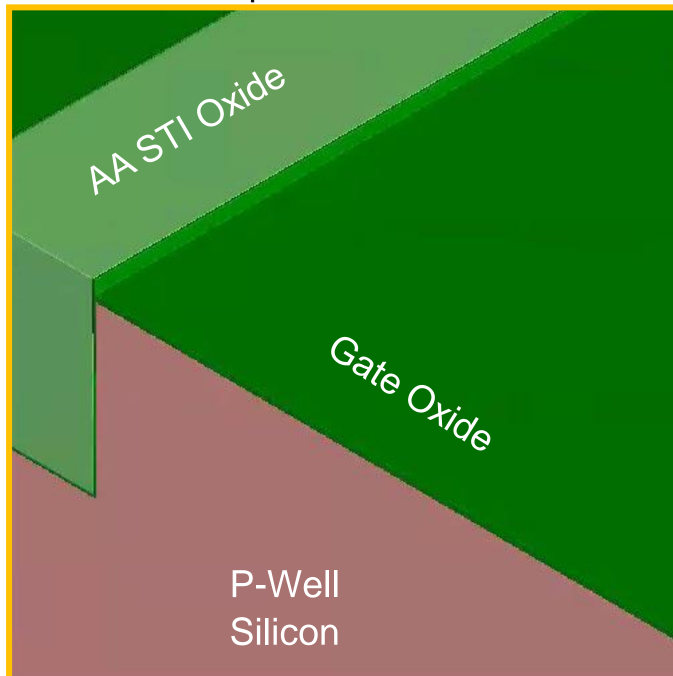


AA STI Oxide
N-Well
P-Well
Silicon Substrate

TG GATE OXIDE GROWTH [DIFFUSION]

- In the **Diffusion Area** a thin film of high-quality silicon dioxide is grown on the surface of the silicon wafer. This oxide will be an important part of the gates of the CMOS transistors: the gate oxide.

Detail Close-up

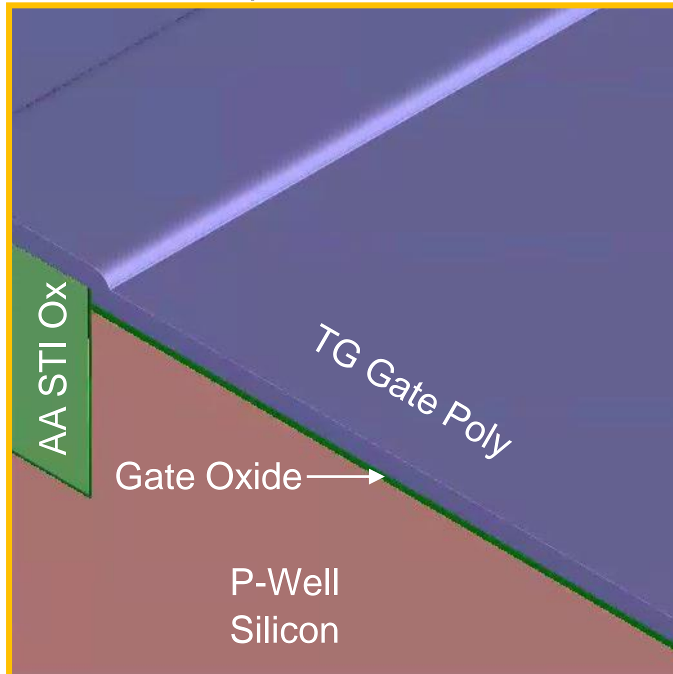


AA STI Oxide
Gate Oxide
N-Well
P-Well
Silicon Substrate

TG GATE POLYSILICON DEPOSITION [DIFFUSION]

- In the **Diffusion Area** a polycrystalline silicon film (known as "poly") is deposited on top of the gate oxide. The poly will be the electrodes of the transistor gates.
- Note: The poly is doped N-type or P-type, shown as purple (N-type) or pink (P-type) in the diagram, as needed for optimal performance of the CMOS devices. The doping will be accomplished by a series of implants (not described in this document).

Detail Close-up

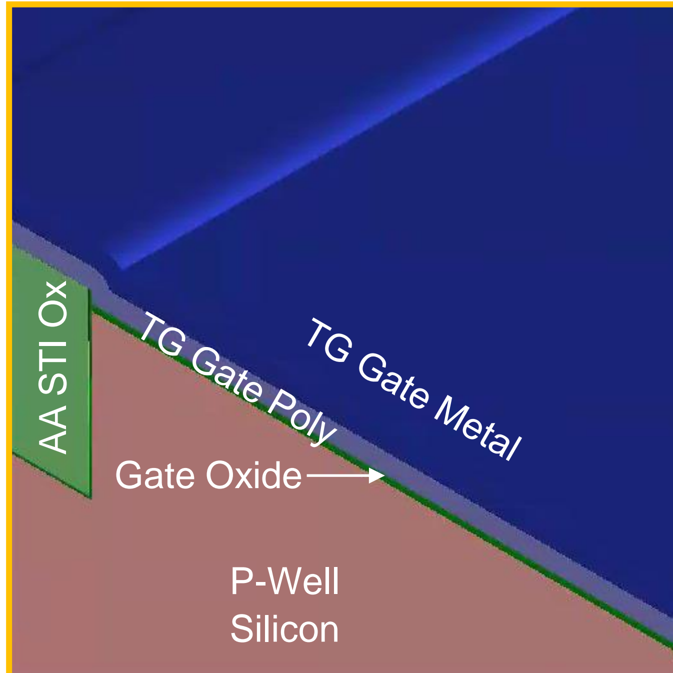


TG Gate Poly
STI Ox
N-Well
P-Well
Silicon Substrate

TG GATE METAL DEPOSIT
[PHYSICAL VAPOR DEPOSITION (PVD)]

- In the **PVD Area** a metal film is deposited on top of the polysilicon film. This will form the conductive part of the transistor gates.
- Note: Several different types of metals may be used for this step

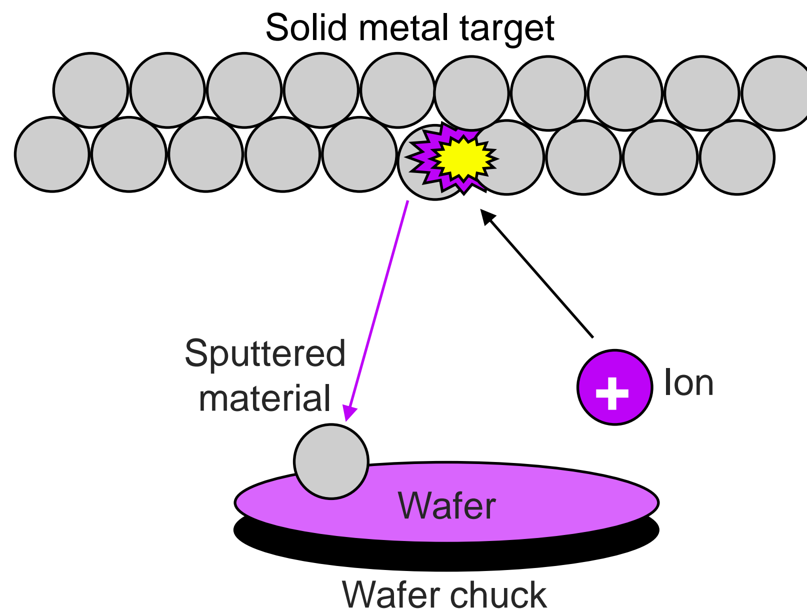
Detail Close-up

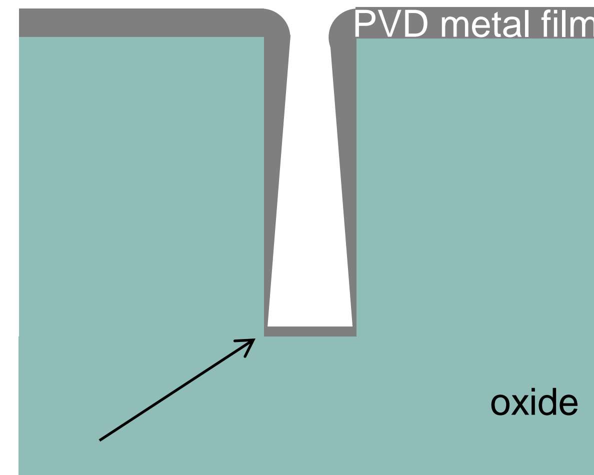


Physical Vapor Deposition (PVD)

- Many of the metal films in the process are deposited using Physical Vapor Deposition (PVD) technology (also known as "sputtering").
- Ions bombard a metal target. The sputtered metal deposits on the wafer.
- The process involves little or no chemistry, and takes place at low (or room) temperature.
- PVD deposits a wide variety of metal films quickly and at relatively low cost.
- PVD films do not deposit as conformally as CVD films, so they cannot be used to fill deep contacts or trenches.

Typical PVD Process





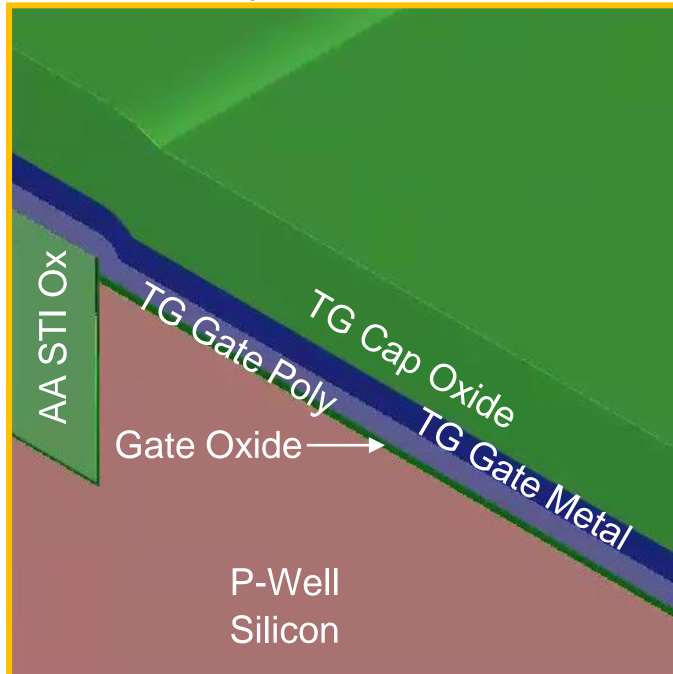
PVD Metal Thinning at the Bottom of a Deep Contact

Compare with CVD

TG CAP OXIDE DEPOSIT [CVD]

- In the **CVD Area** a thick film of silicon dioxide is deposited to protect the gate metal layer from corrosion and damage.
- Note: Some technologies use silicon nitride for this purpose.
  - This film is called Cap Oxide in this case.

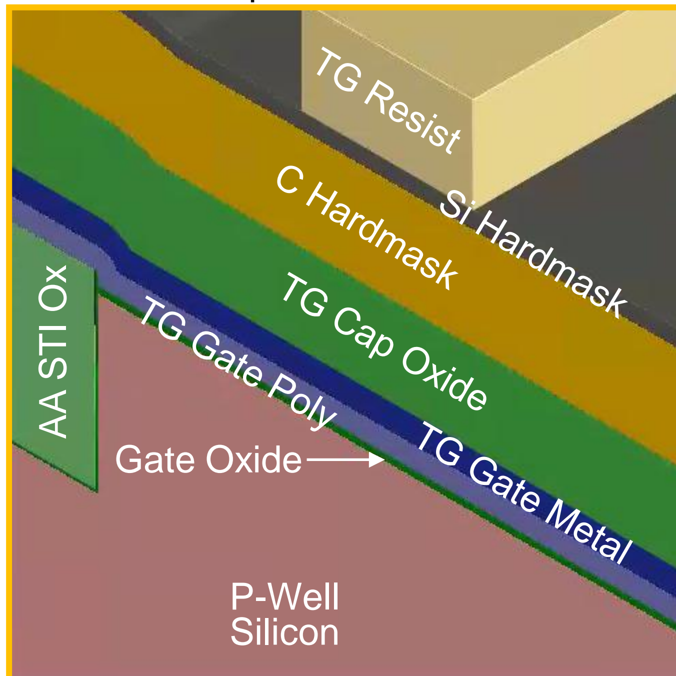
Detail Close-up



TG HARDMASK LAYERS DEPOSIT

- Deposit hardmask layers for patterning the transistor gates.

Detail Close-up



TG GATE PHOTO PATTERN

- The “TG” mask is used to define the pattern in photoresist for the gates of the CMOS devices. The pattern also electrically connects the transistor gates to each other.

3D model shown after photo step

TG Gate Resist

STI Ox

N-Well

P-Well

Silicon Substrate

TG HARDMASK DRY ETCH

- A plasma process is used to transfer the TG photoresist pattern into the underlying hardmask layers.

TG GATE DRY ETCH

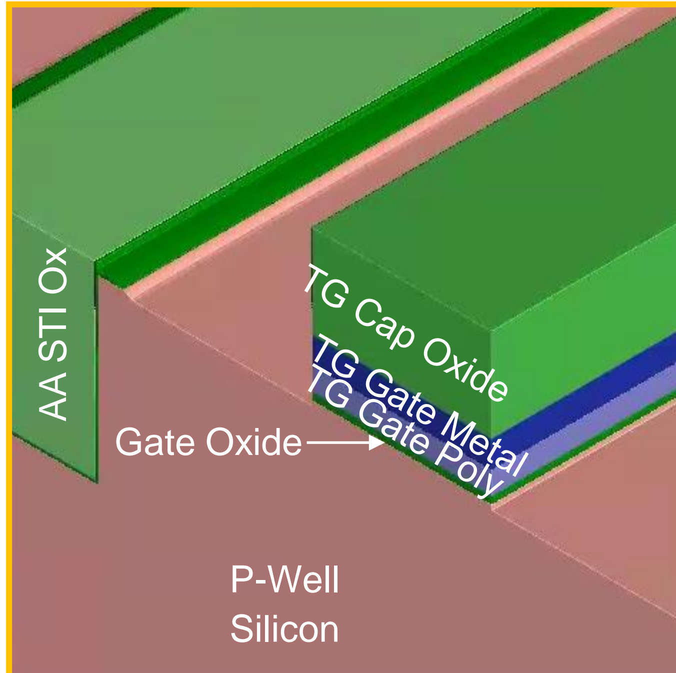
- A second plasma process is used to etch away the unwanted gate stack layers, leaving behind the gates.

TG RESIST STRIP [WET PROCESS]

- Plasma and wet chemistry are used to remove the remaining carbon after the gate etch is complete.

3D model shown after strip step

Detail Close-up

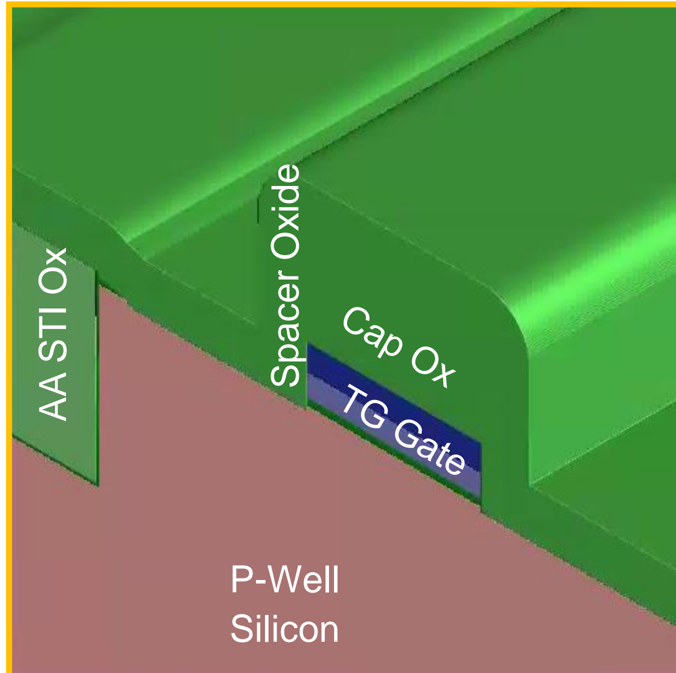


TG Cap Oxide
STI Ox
N-Well
P-Well
Silicon Substrate

TG SPACER OXIDE DEPOSIT [CVD]

- A thin film of silicon dioxide is deposited to form a spacer on the sidewalls of the gate. The spacer will protect the gate metal from corrosion and is used to ensure the source/drain implants will be correctly aligned to the gate.

Detail Close-up

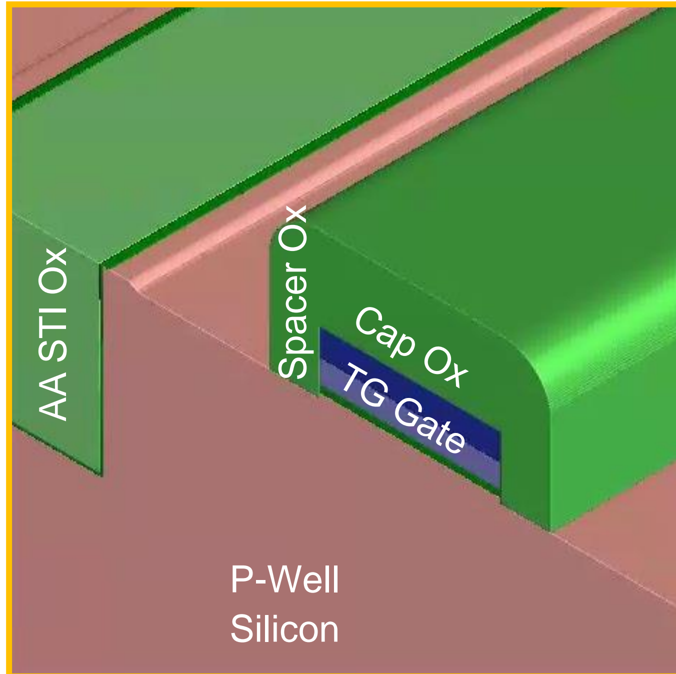


Spacer Oxide
STI Ox
N-Well
P-Well
Silicon Substrate

TG SPACER OXIDE DRY ETCH [DRY ETCH]

- A specially-designed plasma process is used to etch the spacer oxide from the horizontal surfaces while the oxide remains intact on the sidewalls of the gates.

Detail Close-up



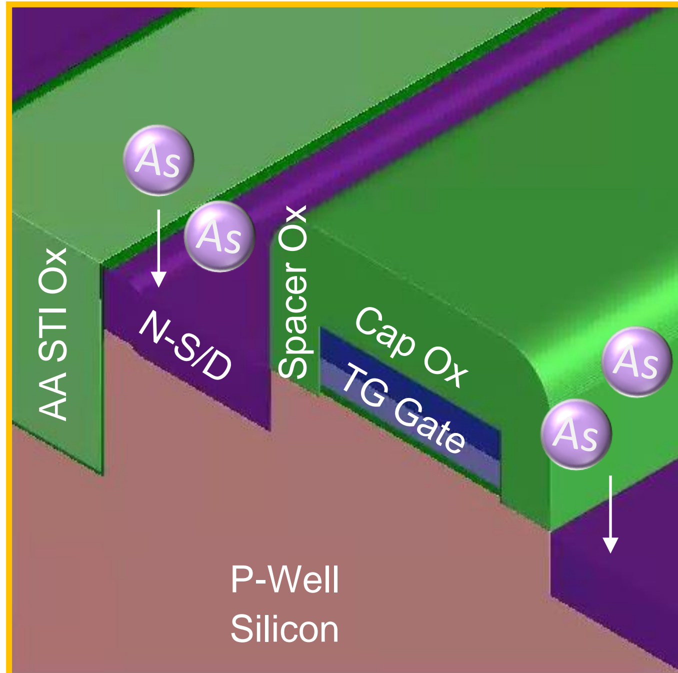
Spacer Oxide
STI Ox
N-Well
P-Well
Silicon Substrate

NA N-SOURCE/DRAIN PHOTO PATTERN

- The “NA” mask opens up the NMOS transistors to receive the N source/drain implant. A thick resist is used to block the implant in the areas that should not receive the implant.

NA N-SOURCE/DRAIN IMPLANT

- An ion implanter shoots a high dose of arsenic ions into the silicon near the surface to form the sources and drains of the NMOS transistors.
- Note: The gate and spacers confine the implant to the S/D regions only. This is known as a “self-aligned” implant.



NA RESIST STRIP [WET PROCESS]

- Plasma and wet chemistry are used to remove the photoresist after the implant is complete

3D model shown before resist strip

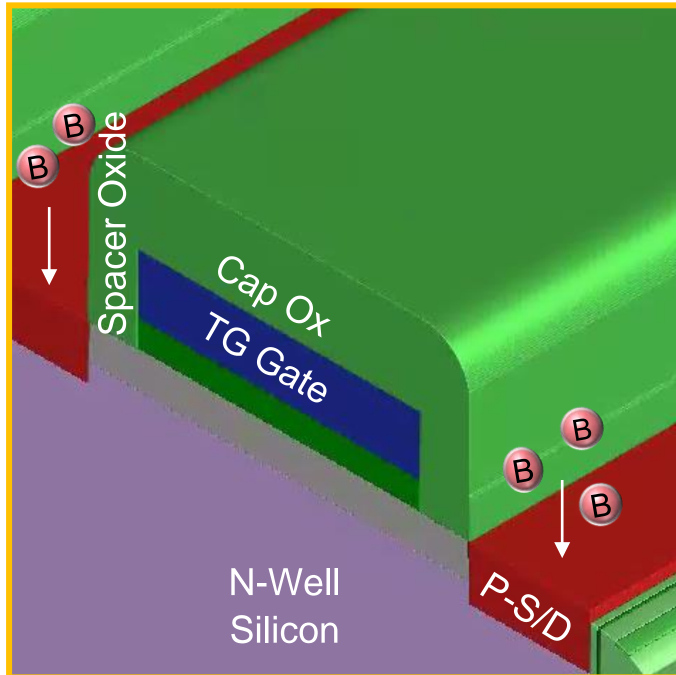
NA Resist
STI Ox
N-Source/Drain
Spacer Oxide
N-Well
P-Well
Silicon Substrate

PA P-SOURCE/DRAIN PHOTO PATTERN

- The “PA” mask opens up the PMOS transistors to receive the P source/drain implant. A thick resist is used to block the implant in the areas that should not receive the implant.

PA P-SOURCE/DRAIN IMPLANT

- An ion implanter shoots a high dose of boron ions into the silicon near the surface to form the sources and drains of the PMOS transistors.
- Note: The gate and spacers confine the implant to the S/D regions only. This is known as a “self-aligned” implant.



PA RESIST STRIP [WET PROCESS]

- Plasma and wet chemistry are used to remove the photoresist after the implant is complete.

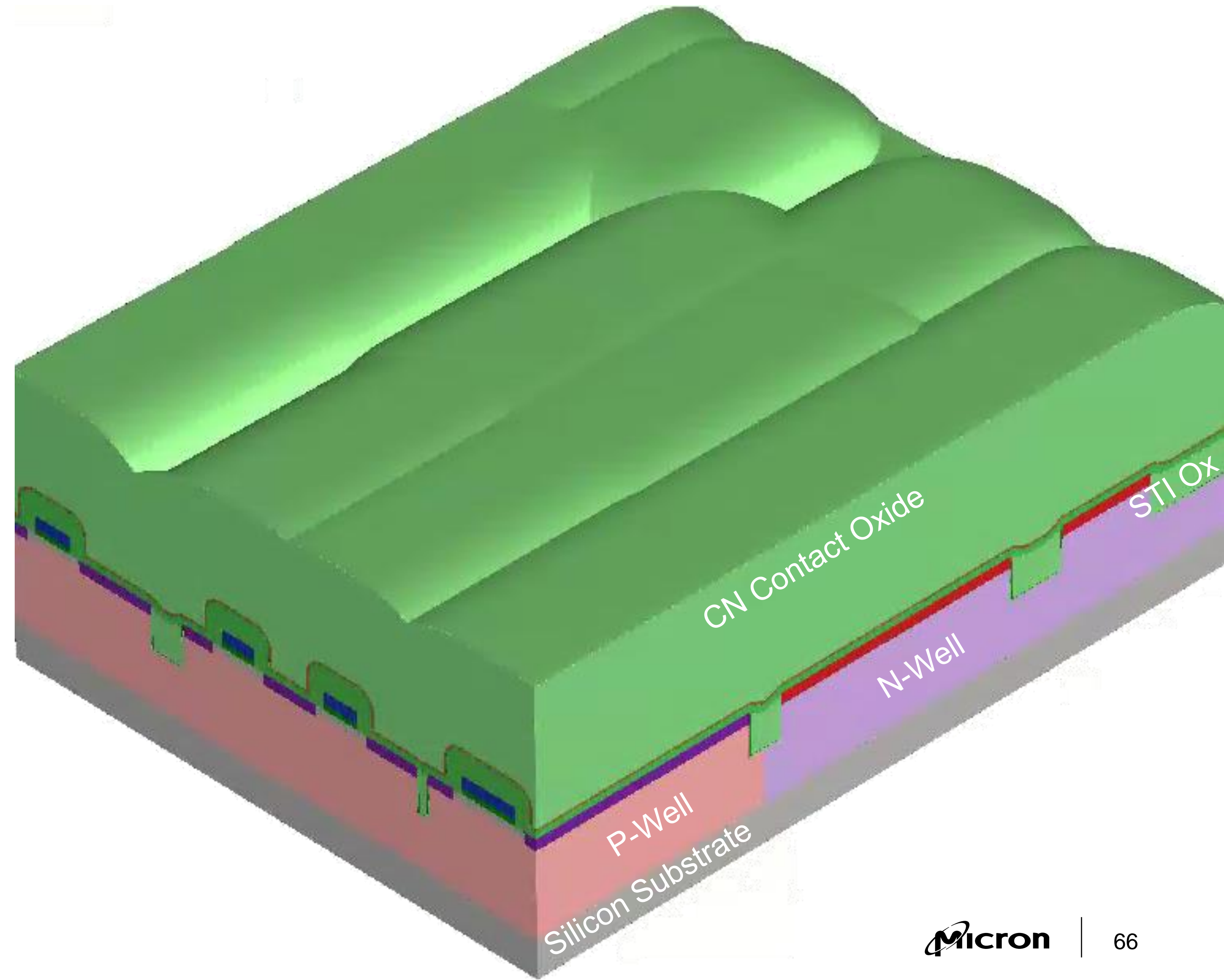
3D model shown before resist strip

PA Resist
Spacer Oxide
STI Ox
P-Source/Drain
P-Well
N-Well
Silicon Substrate

CN CONTACT OXIDE DEPOSIT [CVD]

- A thick film of silicon dioxide is deposited to protect the CMOS transistors.

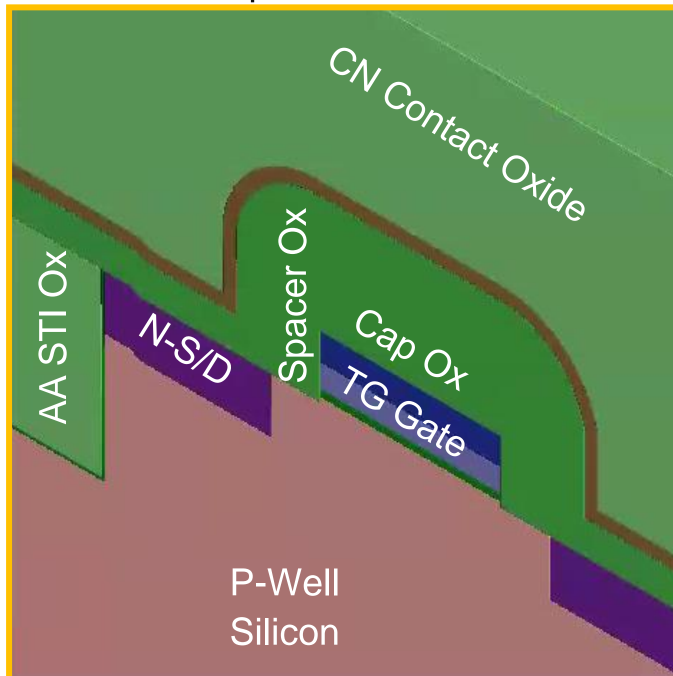
Q) What do you think is the next Traveler step?



CN CONTACT OXIDE CMP [CMP]

- A polishing process is used to planarize the wafer surface to improve photo patterning of contacts. In this case a CMP “Stop in Film” timed process is used.

Detail Close-up

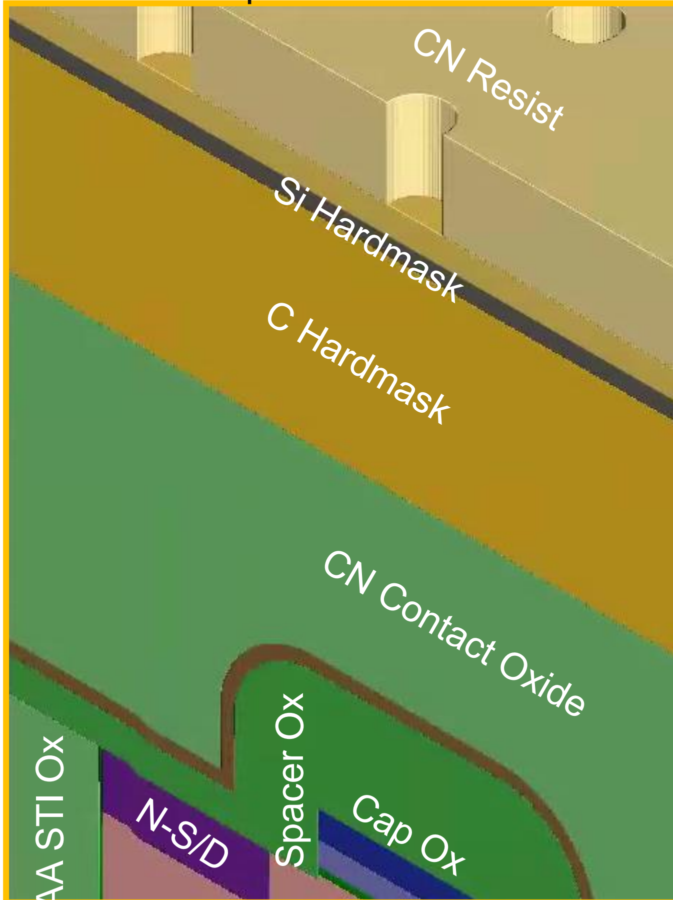


CN Contact Oxide
STI Ox
N-Well
P-Well
Silicon Substrate

CN HARDMASK LAYERS DEPOSIT

- Deposit hardmask layers for patterning the contacts.

Detail Close-up



CN CONTACT PHOTO PATTERN

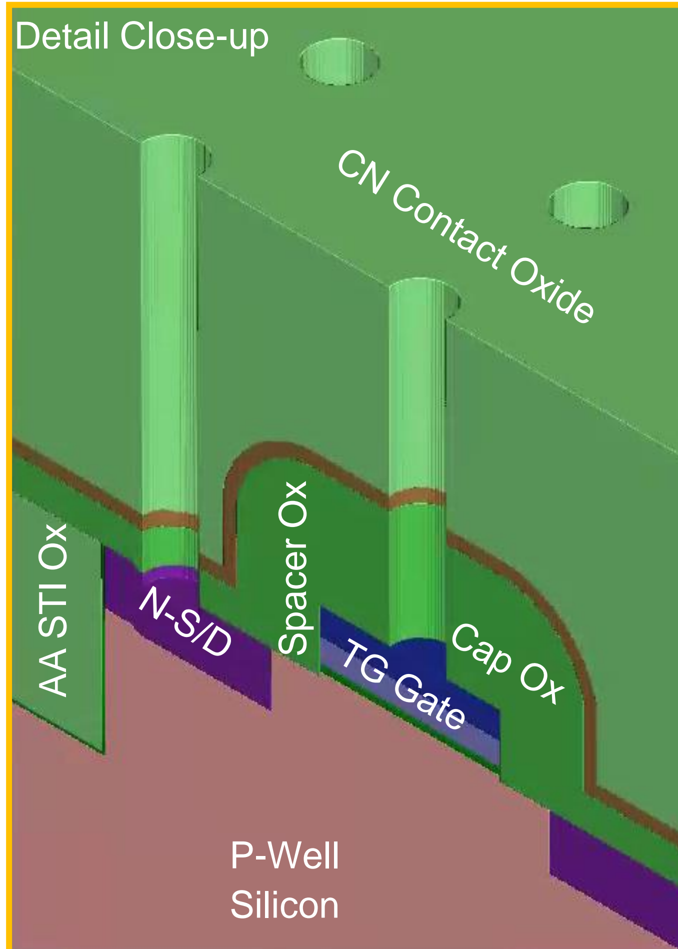
- The "CN" mask is used to define the pattern in photoresist for the contacts. The contacts will provide vertical conductive paths (wires) from the CMOS devices to the first interconnect level.

3D model shown after photo step

CN Resist
CN Contact Oxide
STI Ox
N-Well
P-Well
Silicon Substrate

CN CONTACT DRY ETCH

- A plasma process is used to etch holes in the hardmask layers, and down through the oxide films. The etch has selectivity to stop on the sources and drains (silicon), and gates (metal).



CN RESIST STRIP [WET PROCESS]

- Plasma and wet chemistry are used to remove the remaining carbon after the contact etch is complete.

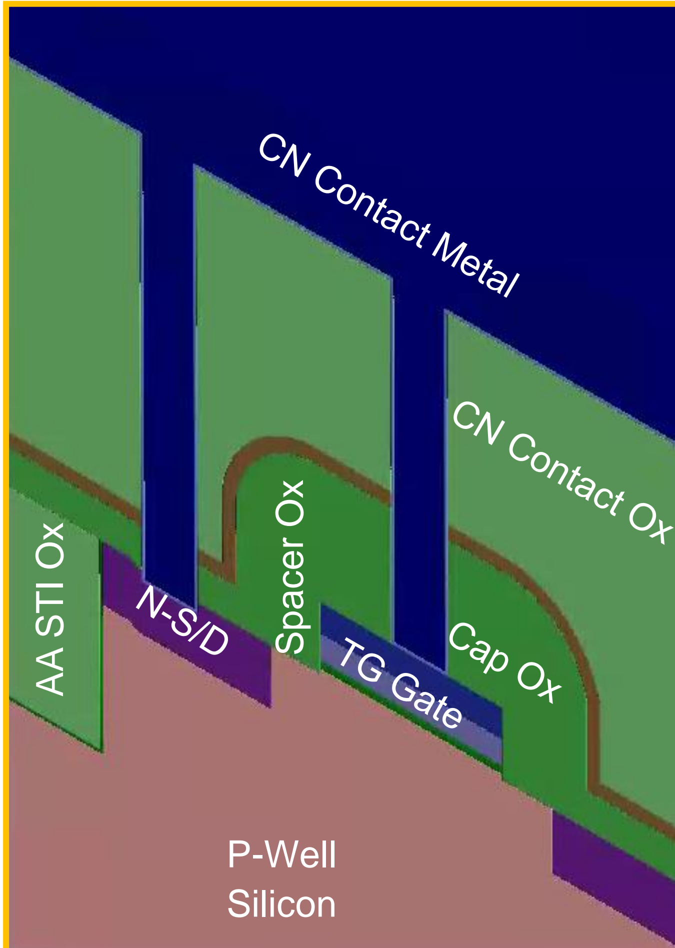
3D model shown after hardmask strip

CN Contact Oxide
STI Ox
N-Well
P-Well
Silicon Substrate

CN CONTACT METAL DEPOSIT [CVD]

- A conductive metal layer is deposited to fill the contact holes. CVD tungsten (W) is chosen to completely fill the holes without creating voids.

Detail Close-up

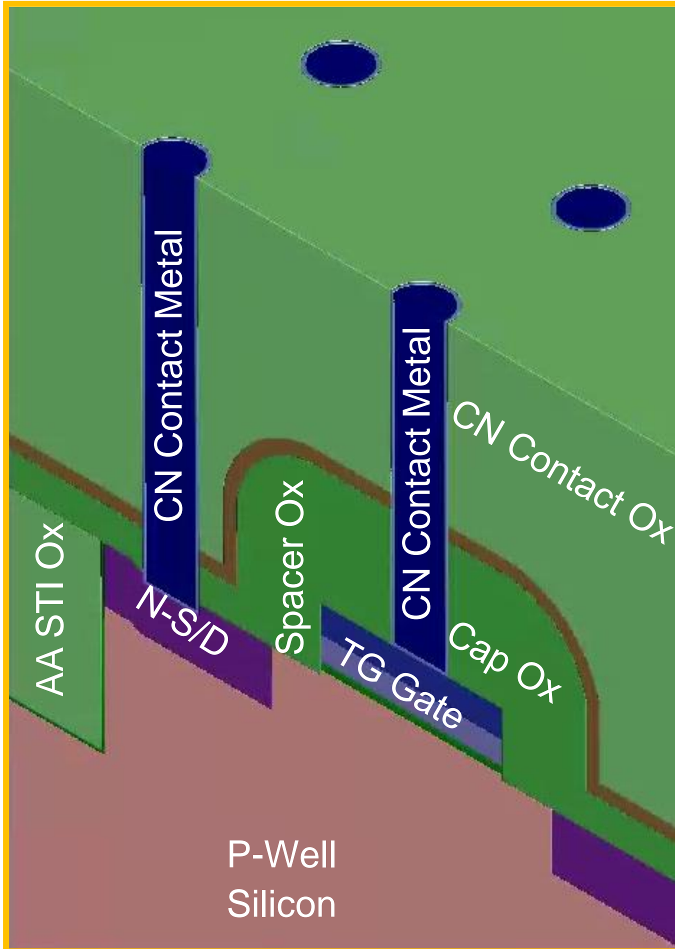


Q) What do you think is the next Traveler step?

CN CONTACT METAL CMP [CMP]

- A polishing process is used to remove all of the metal on the surface (known as “overburden”), leaving only the contacts filled with metal.

Detail Close-up



Q) What do you think is the next Traveler step?

CN Contact Metal

STI Ox

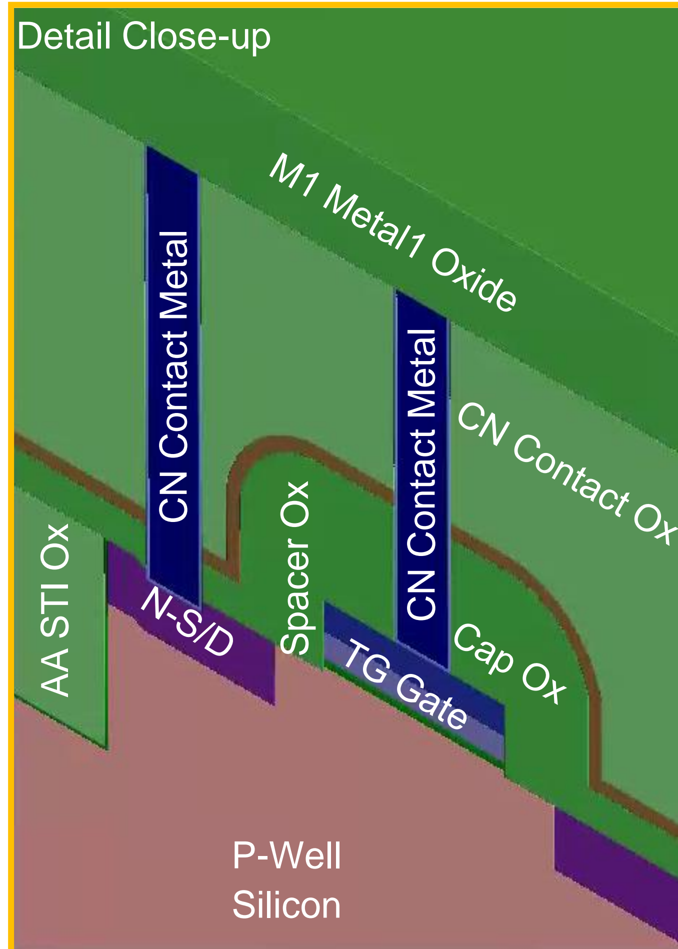
N-Well

P-Well

Silicon Substrate

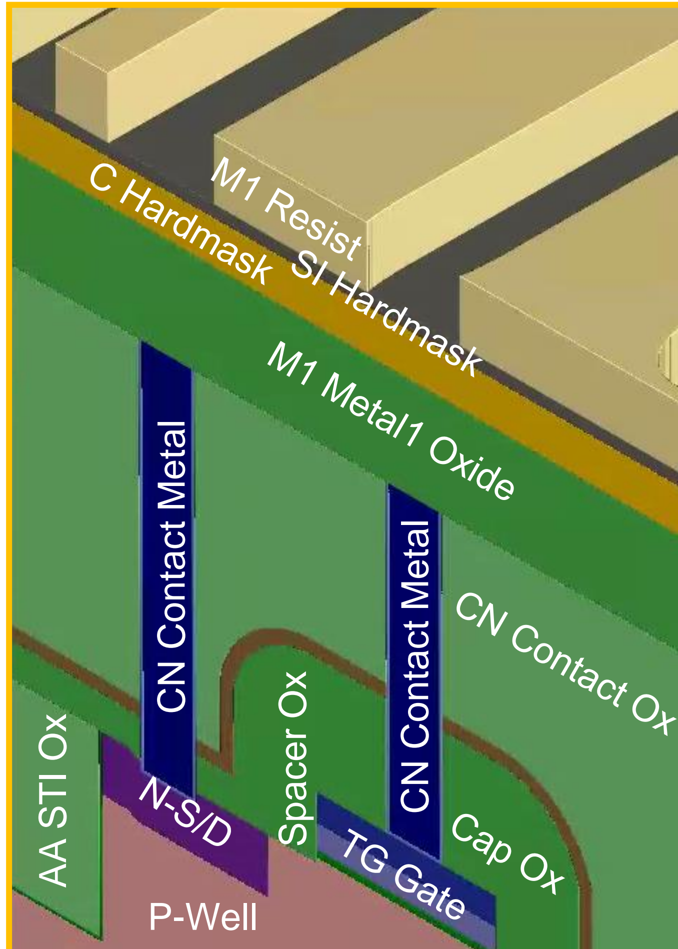
M1 METAL1 OXIDE DEPOSIT [CVD]

- A thick film of silicon dioxide is deposited to serve as the foundation for the formation of the first metal interconnect layer.
- Note: Most chips will have multiple levels of metal interconnects. In this example, we will only show one level.



M1 HARDMASK LAYERS DEPOSIT

- Deposit hardmask layers for patterning the metal interconnects.



M1 METAL1 PHOTO PATTERN

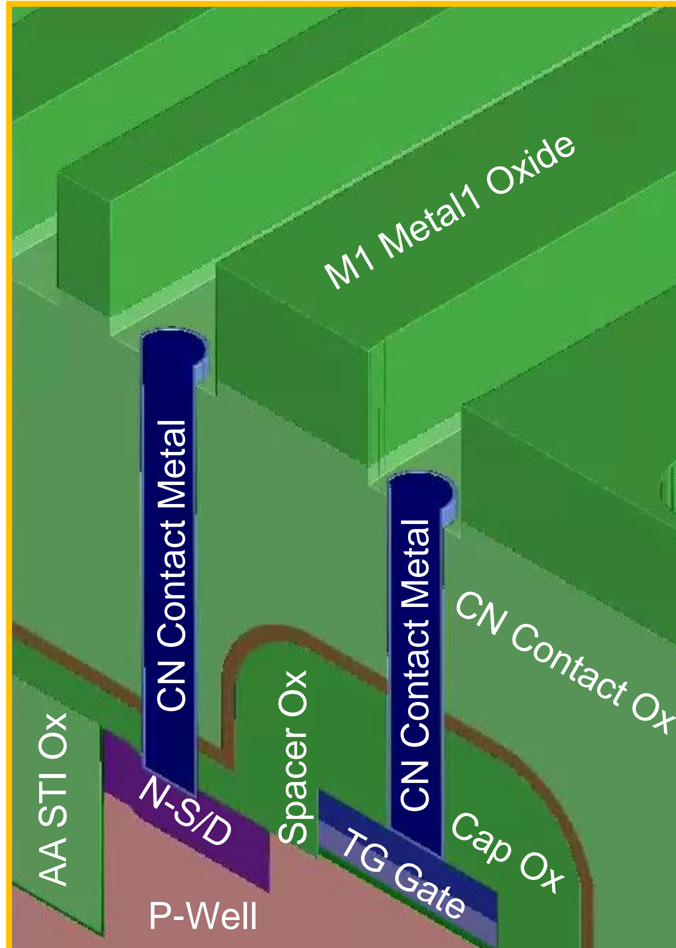
- The “M1” mask is used to define the pattern in photoresist for the first level of metal interconnects. The interconnects will provide horizontal conductive paths (wires) connecting the various parts of the circuit.

3D model shown after photo step

M1 METAL1 DRY ETCH

- A plasma process is used to etch trenches in the M1 oxide layer. The etch must be deep enough to expose the top of the CN metal contacts.

Detail Close-up



M1 RESIST STRIP [WET PROCESS]

- Plasma and wet chemistry are used to remove the remaining carbon after the trench etch is complete.

Q) What do you think is the next Traveler step?

3D model shown after resist strip

M1 Metal1 Oxide

STI Ox

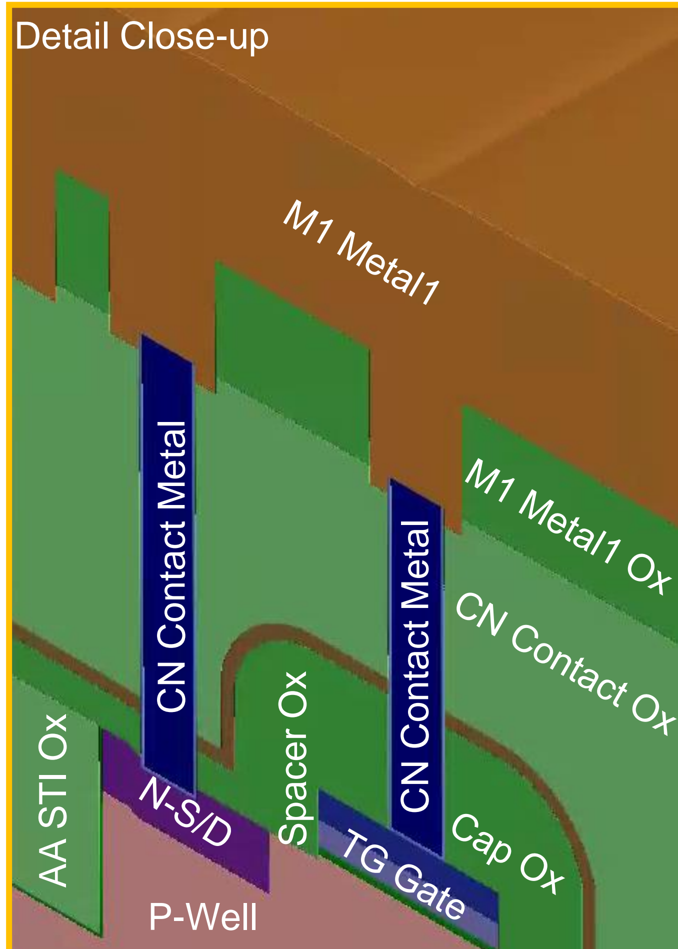
N-Well

P-Well

Silicon Substrate

M1 METAL1 METAL DEPOSIT [WET PROCESS]

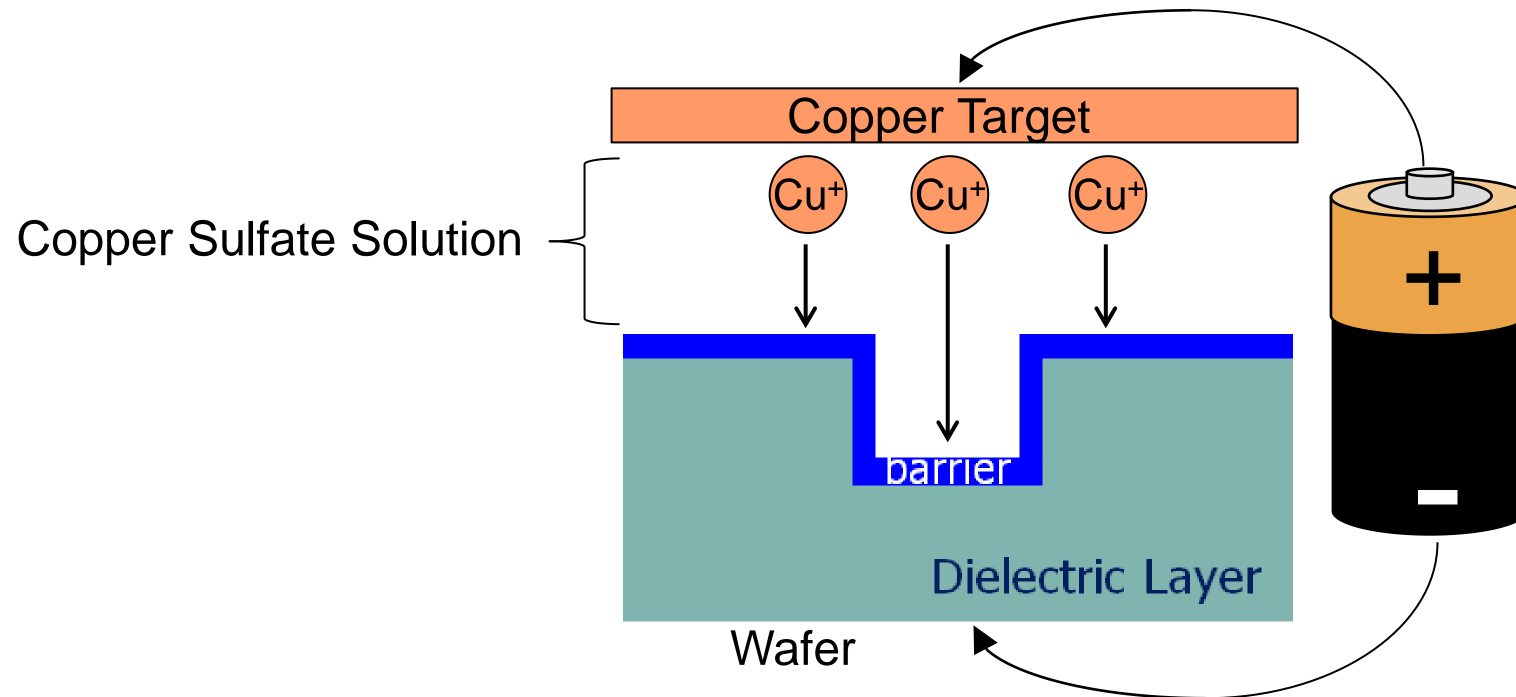
- A conductive metal layer is deposited to fill the trenches. Copper (Cu) is chosen for low resistivity. A special wet chemical process known as “electroplating” is used to deposit the copper.



M1 Metal1
STI Ox
N-Well
P-Well
Silicon Substrate

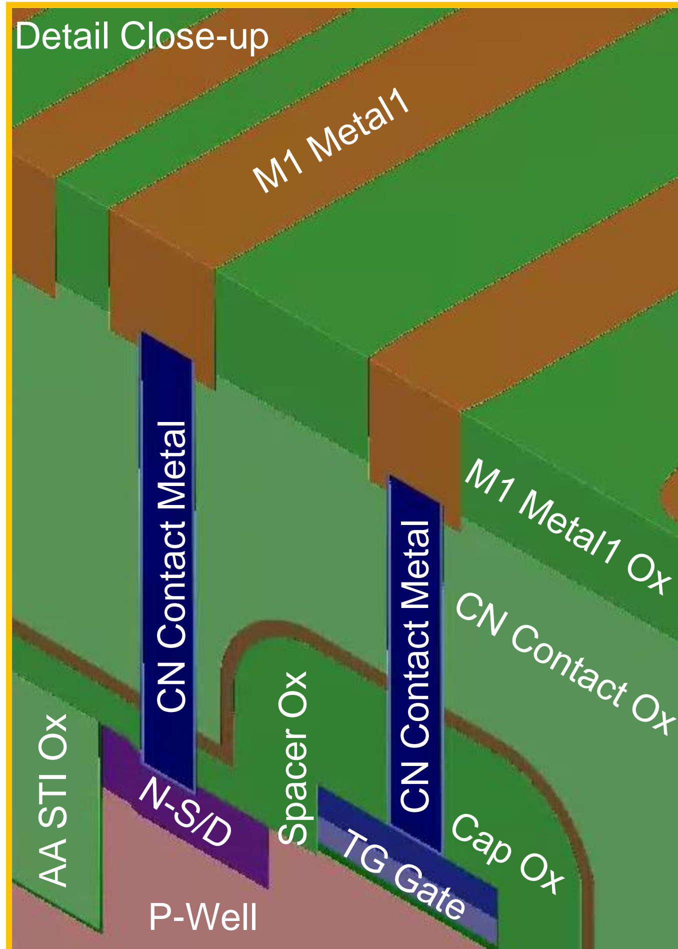
Wet Process – Electroplating

- Copper is uniquely deposited via electroplating.
- The wafer is immersed in a solution of copper sulfate. An electric current is forced through the solution, and copper ions are transported from a target to the wafer.
- Electroplating effectively fills deep trenches and is more cost effective than PVD for thick copper layers.



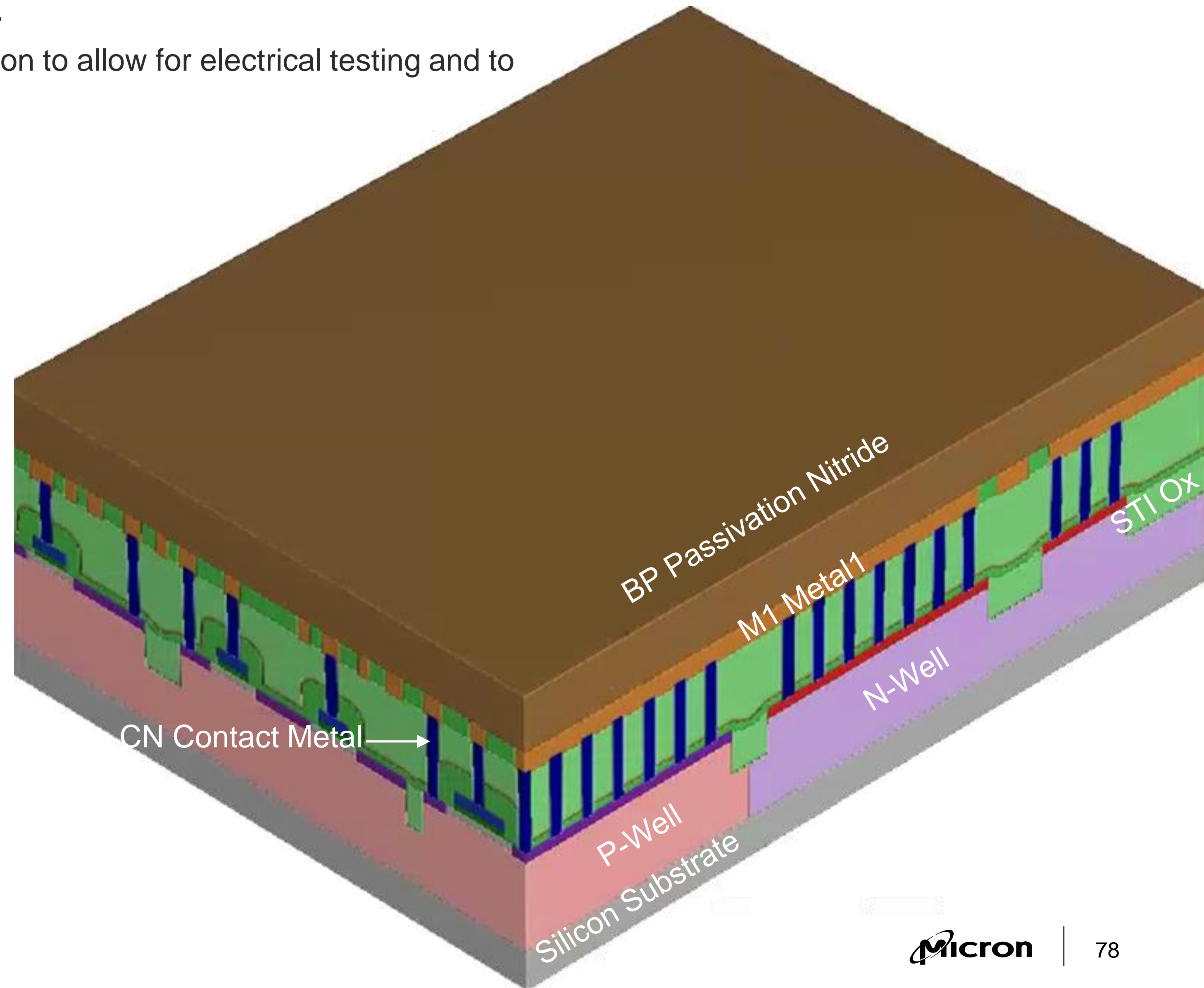
M1 METAL1 CMP [CMP]

- A polishing process is used to remove all of the overburden metal on the surface, leaving the trenches filled with copper.
- Note: The process of forming metal interconnects by filling trenches with metal and then using CMP to remove the surface metal is known as “damascene”. (Due to resembling the ancient metal handicrafts made in Damascus, Syria)



BP PASSIVATION DEPOSIT [CVD]

- A thick film of silicon nitride, known as “passivation”, is deposited to protect the fragile circuits and devices from moisture, contamination, and damage.
- Large holes (not shown) will be etched into the passivation to allow for electrical testing and to connect the die circuits to the package.



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