# Technical Note

## Migrating Micron's N25Q 3V, 128Mb, Parameter Blocks Serial Flash Devices to Uniform Subsector Erase Devices

## Introduction

This technical note explains how to migrate from the Micron® N25Q 3V, 128Mb parameter blocks serial NOR Flash device to the N25Q 3V, 128Mb uniform subsector erase serial NOR Flash device. Features compared include memory organization, package options, signal descriptions, the software command set, performance, and block protection.

The device supports legacy SPI protocol(s) as well as the latest quad I/O or dual I/O SPI protocol. It is manufactured using Micron's 65nm technology and provides a minimum of 100,000 PROGRAM/ERASE cycles per sector, with 20-year data retention.

The device uses a single supply voltage from 2.7V to 3.6V and is offered in the industrial temperature range (–40°C to +85°C). Maximum clock frequency is 108 MHz (quad/dual I/O instructions result in an equivalent clock frequency up to 432 MHz). The primary difference between the two devices is in memory organization: parameter blocks devices offer 4KB subsector granularity in the 8 boot sectors (bottom or top parts), and uniform subsector erase devices provide 4KB subsector granularity in the entire memory array.

# Memory Array Architecture

### Table 1: Device Comparison

| Parameter Block Features | Uniform Subsector Erase Features |
|---|---|
| 16,777,216 bytes (8 bits each) | 16,777,216 bytes (8 bits each) |
| 256 sectors (64KB each) | 256 sectors (64KB each) |
| In bottom and top versions: 8 bottom (top) 64KB boot sectors with 16 subsectors (4KB) and 248 standard 64KB sectors | 4096 subsectors (4KB each) |
| 65,536 pages (256 bytes each) | 65,536 pages (256 bytes each) |
| 64 OTP bytes located outside the main memory array | 64 OTP bytes located outside the main memory array |

# Part Number Ordering and Package Configurations

### Table 2: Package Configurations

| Package[1] | JEDEC Name | Package Code | Parameter Blocks | Uniform Subsector Erase |
|---|---|---|---|---|
| VDFPN8 (8mm x 6mm MLP8) | V-PDFN-8/8mm x 6mm | F8 | Yes | Yes |
| TBGA24 (6mm x 8mm AT) | T-PBGA-24b05/6mm x 8mm | 12 | Yes | Yes |
| VDFPN8 (6mm x 5mm Sawn MLP) | V-PDFN-8/6mm x 5mm (Sawn) | F7 | – | Yes |
| SO16 (300 mils body width) | SOP2-16/300 mil | SF | Yes | Yes |
| SO8W (SO8 208 mils body width) | SOP2-8/208 mil | SE | – | Yes |

Note: 1. All packages are RoHS-compliant.

**Table 3: Part Number Cross Reference: 2.7–3.6V**

| Original CP[1] | Package | Equivalent Part Number[1] | Note |
|---|---|---|---|
| N25Q128A13B1240x | T-PBGA-24b05/6mm x 8mm (TBGA 24) | N25Q128A13E1240x | |
| N25Q128A13B1241x | T-PBGA-24b05/6mm x 8mm (TBGA 24) | N25Q128A13E1241x | |
| N25Q128A13BF840x | V-PDFN-8/8mm x 6mm (MLP 8x6) | N25Q128A13EF840x | |
| N25Q128A13BSE40x | SOP2-8/208mil (SO8W) | N25Q128A13ESE40x | |
| N25Q128A13BSF40x | SOP2-16/300mil (SO16W) | N25Q128A13ESF40x | |
| N25Q128A13B1242x | T-PBGA-24b05/6mm x 8mm (TBGA 24) | N25Q128A13E1242x | |
| N25Q128A13BF740x | V-PDFN-8/6mm x 5mm (MLP 6mm x 5mm) (Sawn) | N25Q128A13EF740x | |
| N25Q128A13TF840x | V-PDFN-8/8mm x 6mm (MLP 8mm x 6mm) | N25Q128A13EF840x | |
| N25Q128A13TSF40x | SOP2-16/300mil (SO16W) | N25Q128A13ESF40x | |
| N25Q128A13T1240x | T-PBGA-24b05/6mm x 8mm (TBGA 24) | N25Q128A13E1240x | |
| N25Q128A23BF840x | V-PDFN-8/8mm x 6mm (MLP 8mm x 6mm) | N25Q128A13EF840x | 2 |
| N25Q128A23BSF40x | SOP2-16/300mil (SO16W) | N25Q128A13ESF40x | 2 |
| N25Q128A23B1240x | T-PBGA-24b05/6mm x 8mm (TBGA 24) | N25Q128A13E1240x | 2 |
| N25Q128A23B1241x | T-PBGA-24b05/6mm x 8mm (TBGA 24) | N25Q128A13E1241x | 2 |
| N25Q128A23T1240x | T-PBGA-24b05/6mm x 8mm (TBGA 24) | N25Q128A13E1240x | 2 |
| N25Q128A23TF840x | V-PDFN-8/8mm x 6mm (MLP 8mm x 6mm) | N25Q128A13EF840x | 2 |
| N25Q128A23TSF40x | SOP2-16/300mil (SO16W) | N25Q128A13ESF40x | 2 |
| N25Q128A43BSE40x | SOP2-8/208mil (SO8W) | N25Q128A13ESE40x | 2 |

Notes:
1. Applies to all part numbers: Packing information details: E = tray; F = tape-and-reel; G = tube (16th digit of part number).
2. Basic XIP application should use Micron XIP mode without any software change. Contact your local Micron sales representative for more information.

# Signal Descriptions

### Table 4: Signal Descriptions

Both devices share the same signals and functions

| Parameter Blocks Signal | Uniform Subsector Erase Signal | Type | Description |
|---|---|---|---|
| C | C | Input | Serial clock |
| DQ0 | DQ0 | I/O | Serial data input |
| DQ1 | DQ1 | I/O | Serial data output |
| S# | S# | Input | Chip select |
| W/$V_{PP}$/DQ2 | W/$V_{PP}$/DQ2 | I/O | Write protect/enhanced program supply voltage/additional data I/O |
| HOLD#/DQ3 | HOLD#/DQ3 | I/O | HOLD (RESET function available upon customer request)/additional data I/O |
| $V_{CC}$ | $V_{CC}$ | Power | Supply voltage |
| $V_{SS}$ | $V_{SS}$ | Ground | Ground |

Notes:
1. DQ0, DQ1, DQ2, and DQ3 become I/O signals according to the protocol used.
2. W is used for hardware write protection: the protected area size is defined by nonvolatile bits (BP0, BP1, BP2, BP3, and TB bit). Also, a software write protection is applicable to every 64KB sector (volatile lock bit) and additional smart protections are available upon customer request.
3. HOLD# is used to pause any serial communications with the device without deselecting the device.
4. Reset functionality, rather than hold, is present in devices with a dedicated part number.

# Commands

The parameter blocks device has a fast power-on reset feature to speed up the poweron sequence for applications that only require reading the memory after the power-on sequence (no modify commands). The uniform subsector erase device does not include the fast power-on reset feature.

In dual I/O and quad I/O protocols, the command set is the same for both devices; see the respective data sheets for details.

### Table 5: Extended SPI Protocol Supported Command Set

| Command | Code | Address Bytes | Dummy Clock Cycles | Data Bytes | Notes |
|---|---|---|---|---|---|
| **READ Operations** | | | | | |
| READ IDENTIFICATION | 9Eh/9Fh | 0 | 0 | 1 to 20 | |
| READ | 03h | 3 | 0 | 1 to ∞ | 1 |
| FAST READ | 0Bh | 3 | 8 | 1 to ∞ | 1 |
| DUAL OUTPUT FAST READ | 3Bh | 3 | 8 | 1 to ∞ | 1 |

**Table 5: Extended SPI Protocol Supported Command Set (Continued)**

| Command | Code | Address Bytes | Dummy Clock Cycles | Data Bytes | Notes |
|---|---|---|---|---|---|
| DUAL INPUT/OUTPUT FAST READ | BB | 3 | 8 | 1 to ∞ | 1 |
| QUAD OUTPUT FAST READ | 6Bh | 3 | 8 | 1 to ∞ | 1 |
| QUAD INPUT/OUTPUT FAST READ | EBh | 3 | 10 | 1 to ∞ | 1 |
| READ OTP | 4Bh | 3 | 8 | 1 to 65 | 1 |
| READ SERIAL FLASH DISCOVERY PARAMETER | 5Ah | 3 | 9 | 1 to ∞ | 2 |
| **WRITE Operations** | | | | | |
| WRITE ENABLE | 06h | 0 | 0 | 0 | |
| WRITE DISABLE | 04h | 0 | 0 | 0 | |
| **PROGRAM Operations** | | | | | |
| PAGE PROGRAM | 02h | 3 | 0 | 1 to 256 | |
| DUAL INPUT FAST PROGRAM | A2h | 3 | 0 | 1 to 256 | |
| DUAL INPUT EXTENDED FAST PROGRAM | D2h | 3 | 0 | 1 to 256 | |
| QUAD INPUT FAST PROGRAM | 32h | 3 | 0 | 1 to 256 | |
| QUAD INPUT EXTENDED FAST PROGRAM | 12h | 3 | 0 | 1 to 256 | |
| PROGRAM OTP | 42h | 3 | 0 | 1 to 65 | |
| **ERASE Operations** | | | | | |
| BULK ERASE | C7h | 0 | 0 | 0 | |
| SECTOR ERASE | D8h | 3 | 0 | 0 | |
| SUBSECTOR ERASE | 20h | 3 | 0 | 0 | 3 |
| **SUSPEND Operations** | | | | | |
| PROGRAM/ERASE SUSPEND | 75h | 0 | 0 | 0 | |
| PROGRAM/ERASE RESUME | 7Ah | 0 | 0 | 0 | |
| **REGISTER Operations** | | | | | |
| READ STATUS REGISTER | 05h | 0 | 0 | 1 to ∞ | |
| WRITE STATUS REGISTER | 01h | 0 | 0 | 1 | |
| READ LOCK REGISTER | E8h | 3 | 0 | 1 to ∞ | |
| WRITE LOCK REGISTER | E5h | 3 | 0 | 1 | |
| READ FLAG STATUS REGISTER | 70h | 0 | 0 | 1 to ∞ | |
| CLEAR FLAG STATUS REGISTER | 50h | 0 | 0 | 0 | |
| READ NONVOLATILE CONFIGURATION REGISTER | B5h | 0 | 0 | 2 | |
| WRITE NONVOLATILE CONFIGURATION REGISTER | B1h | 0 | 0 | 2 | |
| READ VOLATILE CONFIGURATION REGISTER | 85h | 0 | 0 | 1 to ∞ | |
| WRITE VOLATILE CONFIGURATION REGISTER | 81h | 0 | 0 | 1 | |

**Table 5: Extended SPI Protocol Supported Command Set (Continued)**

| Command | Code | Address Bytes | Dummy Clock Cycles | Data Bytes | Notes |
|---|---|---|---|---|---|
| READ ENHANCED VOLATILE CONFIGURATION REGISTER | 65h | 0 | 0 | 1 to ∞ | |
| WRITE ENHANCED VOLATILE CONFIGURATION REGISTER | 61h | 0 | 0 | 1 | |

Notes:
1. The number of dummy clock cycles is configurable by the user.
2. Command applies to the uniform subsector erase device only.
3. For the parameter blocks device, the SUBSECTOR ERASE command is available only in the bottom or top part of the memory array. For the uniform subsector erase device, the SUBSECTOR ERASE command is available for all sectors of the entire memory array.

**Table 6: RESET Command Codes**

The following commands are supported only on the uniform subsector erase device

| Command | Code | Data Bytes |
|---|---|---|
| RESET ENABLE | 66h | 0 |
| RESET MEMORY | 99h | 0 |

Note:
1. The uniform subsector erase device features an additional RESET command code that enables the device to be reset through a dedicated command. Refer to the device data sheet for more information.

# DC Characteristics and Operating Conditions

Parameter blocks and uniform subsector erase devices share the same specifications.

### Table 7: DC Current Characteristics and Operating Conditions

| Parameter | Symbol | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | | – | ±2 | µA |
| Output leakage current | $I_{LO}$ | | – | ±2 | µA |
| Standby current | $I_{CC1}$ | S = $V_{CC}$; $V_{IN}$ = $V_{SS}$ or $V_{CC}$ | – | 100 | µA |
| Operating current (FAST READ – single I/O) | $I_{CC3}$ | C = 0.1$V_{CC}$/0.9$V_{CC}$ at 108 MHz; DQ1 = open | – | 15 | mA |
| | | C = 0.1$V_{CC}$/0.9$V_{CC}$ at 54 MHz; DQ1 = open | | | |
| Operating current (FAST READ –dual I/O) | | C = 0.1$V_{CC}$/0.9$V_{CC}$ at 108 MHz | – | 6 | mA |
| Operating current (FAST READ – quad I/O) | | C = 0.1$V_{CC}$/0.9$V_{CC}$ at 108 MHz | – | 18 | mA |
| Operating current (PAGE PROGRAM – single, dual, quad I/O) | $I_{CC4}$ | S# = $V_{CC}$ | – | 20 | mA |
| Operating current (WRITE STATUS REGISTER) | $I_{CC5}$ | S# = $V_{CC}$ | – | 20 | mA |
| Operating current (SECTOR ERASE) | $I_{CC6}$ | S# = $V_{CC}$ | – | 20 | mA |
| Input low voltage | $V_{IL}$ | | –0.5 | 0.3$V_{CC}$ | V |
| Input high voltage | $V_{IH}$ | | 0.7$V_{CC}$ | $V_{CC}$ + 0.4 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.6mA | – | 0.4 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –100µA | $V_{CC}$ - 0.2 | – | V |

### Table 8: Operating Conditions

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2.7 | 3.6 | V |
| Supply voltage on $V_{PP}$ | $V_{PPH}$ | 8.5 | 9.5 | V |
| Ambient operating temperature | $T_A$ | –40 | 85 | °C |

# AC Characteristics

### Table 9: AC Characteristics

Note 1 applies to entire table

| Parameter | Symbol | Min | Typ[3] | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Clock frequency for all commands other than READ (SPI-ER, QIO-SPI protocol) | $^{f}C$ | DC | – | 108 | MHz | |
| Clock frequency for READ commands | $^{f}R$ | DC | – | 54 | MHz | |
| Clock HIGH time | $^{t}CH$ | 4 | – | – | ns | 2 |
| Clock LOW time | $^{t}CL$ | 4 | – | – | ns | 3 |
| Clock rise time (peak-to-peak) | $^{t}CLCH$ | 0.1 | – | – | V/ns | 5, 4 |
| Clock fall time (peak-to-peak) | $^{t}CHCL$ | 0.1 | – | – | V/ns | 5, 4 |
| S# active setup time (relative to clock) | $^{t}SLCH$ | 4 | – | – | ns | |
| S# not active hold time (relative to clock) | $^{t}CHSL$ | 4 | – | – | ns | |
| Data in setup time | $^{t}DVCH$ | 2 | – | – | ns | |
| Data in hold time | $^{t}CHDX$ | 3 | – | – | ns | |
| S# active hold time (relative to clock) | $^{t}CHSH$ | 4 | – | – | ns | |
| S# not active setup time (relative to clock) | $^{t}SHCH$ | 4 | – | – | ns | |
| S# deselect time after a READ command | $^{t}SHSL1$ | 20 | – | – | ns | |
| S# deselect time after an unsupported READ operation, or any other operation | $^{t}SHSL2$ | 50 | – | – | ns | |
| Output disable time | $^{t}SHQZ$ | – | – | 8 | ns | 4 |
| Clock LOW to output valid under 30pF | $^{t}CLQV$ | – | – | 7 | ns | |
| Clock LOW to output valid under 10pF | | – | – | 5 | ns | |
| Output hold time | $^{t}CLQX$ | 1 | – | – | ns | |
| HOLD command setup time (relative to clock) | $^{t}HLCH$ | 4 | – | – | ns | |
| HOLD command hold time (relative to clock) | $^{t}CHHH$ | 4 | – | – | ns | |
| HOLD command setup time (relative to clock) | $^{t}HHCH$ | 4 | – | – | ns | |
| HOLD command hold time (relative to clock) | $^{t}CHHL$ | 4 | – | – | ns | |
| HOLD command to output Low-Z | $^{t}HHQX$ | – | – | 8 | ns | 4 |
| HOLD command to output High-Z | $^{t}HLQZ$ | – | – | 8 | ns | 4 |
| Write protect setup time | $^{t}WHSL$ | 20 | – | – | ns | 6 |
| Write protect hold time | $^{t}SHWL$ | 100 | – | – | ns | 6 |
| Enhanced program supply voltage HIGH ($V_{PPH}$) to CS# LOW for single and dual I/O page program | $^{t}VPPHSL$ | 200 | – | – | ns | 7 |
| WRITE STATUS REGISTER cycle time | $^{t}W$ | – | 1.3 | 8 | ms | |
| CLEAR FLAG STATUS REGISTER cycle time | $^{t}CFSR$ | – | 40 | – | ns | |
| WRITE NONVOLATILE CONFIGURATION REGISTER cycle time | $^{t}WNVCR$ | – | 0.2 | 3 | s | |
| WRITE VOLATILE CONFIGURATION REGISTER cycle time | $^{t}WVCR$ | – | 40 | – | ns | |

**Table 9: AC Characteristics (Continued)**

Note 1 applies to entire table

| Parameter | Symbol | Min | Typ[3] | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| WRITE VOLATILE ENHANCED CONFIGURATION REGISTER cycle time | $^{t}$WRVECR | – | 40 | – | ns | |

Notes:
1. Both the parameter blocks and uniform subsector erase devices share all but the following specifications:
   - For the uniform subsector erase device, $^{t}$W = 8ms (MAX); for the parameter blocks device, $^{t}$W = 15ms (MAX).
   - For the uniform subsector erase device, $^{t}$WNVCR = 0.2s (TYP) and 3s (MAX); for the parameter blocks device, $^{t}$WNVCR = 1s (TYP) and 15s (MAX).
   - For the uniform subsector erase device, $V_{PPH}$ can be applied to W/$V_{PP}$ during a BULK ERASE operation. (This operation is not supported in the parameter blocks device. See Note 7.)
2. $^{t}$CH + $^{t}$CL must be greater than or equal to 1/$^{f}$C.
3. Typical values given for $T_A$ = 25°C.
4. Value guaranteed by characterization; not 100% tested in production.
5. Expressed as a slew rate.
6. Only applicable as a constraint for a WRITE STATUS REGISTER command when the status register write disable bit is set to 1.
7. $V_{PPH}$ should be kept at a valid level until the PROGRAM or ERASE operation has completed and its result (success or failure) is known.

# Program and Erase Specifications

### Table 10: Program and Erase Specifications

Typical values given for $T_A$ = 25°C

| Parameter | Symbol | Parameter Blocks Device | | Uniform Subsector Erase Device | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | Typ | Max | Typ | Max | | |
| PAGE PROGRAM cycle time (*n* bytes) | $^{t}$PP | Int (n/8) x 0.025 | 5 | Int (n/8) x 0.015 | 5 | ms | 1, 2 |
| PROGRAM OTP cycle time (64 bytes) | | 0.2 | – | 0.2 | – | ms | |
| SUBSECTOR ERASE cycle time | $^{t}$SSE | 150 | 500 | 200 | 2000 | ms | |
| SECTOR ERASE cycle time | $^{t}$SE | 1 | 3 | 0.7 | 3 | s | |
| Sector erase, $V_{PP} = V_{PPH}$ | $^{t}$SE | N/A | N/A | 0.6 | 3 | s | 3 |
| BULK ERASE cycle time | $^{t}$BE | 256 | 700 | 170 | 250 | s | |
| Bulk erase, $V_{PP} = V_{PPH}$ | $^{t}$BE | N/A | N/A | 160 | 250 | s | 3 |

Notes:
1. When using the PAGE PROGRAM command to program consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes (1< n < 256).
2. Int (A) corresponds to the upper integer part of A. For example, int (12/8) = 2, int (32/8) = 4, int (15.3) = 16.
3. On the parameter blocks device, $V_{PPH}$ cannot be applied to W/$V_{PP}$ during sector erase and bulk erase.

# Device Identification

Manufacturer identification is assigned by JEDEC. The device identification is assigned by the manufacturer and indicates the memory type in the first byte and the memory capacity in the second byte. Device identification is the same for both the parameter blocks and uniform subsector erase devices, and command 9Fh is used to read manufacturer ID and memory type codes in both devices.

N25Q has a unique ID composed of 17 read-only bytes, which contain the following data:

- The first byte is set to 10h.
- The next two bytes of extended device ID specify device configuration (uniform architecture, and hold or reset functionality).
- For the parameter blocks device, the next 14 bytes contain optional customized factory data. The customized factory data bytes are factory programmed with customer data upon request or set to 00h. The uniform subsector erase device is already preprogrammed with an unique ID on all versions.

### Table 11: Read Identification Summary

| Parameter | Parameter Blocks and Uniform Subsector Erase Devices |
|---|---|
| **Device ID** | |
| Manufacturer ID | 20h |

**Table 11: Read Identification Summary (Continued)**

| Parameter | Parameter Blocks and Uniform Subsector Erase Devices |
|---|---|
| Memory type | BAh |
| Memory capacity | 18h |
| **Unique ID** | |
| Extended device ID + customized factory data length 10h | 10h |
| Extended device ID 2 bytes | 2 bytes |
| Customized factory data 14 bytes | 14 bytes |

Note: 1. The uniform subsector erase device supports the Serial Flash Discovery Parameter Data Structure table (see device data sheet).

**Table 12: Extended Device ID, First Byte**

Bottom and top (Bit 1 and Bit 0) refer to the parameter blocks devices

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Volatile configuration register, XIP bit setting:<br>0 = Required<br>1 = Not required | HOLD/RESET function:<br>0 = HOLD<br>1 = RESET | Addressing:<br>0 = by byte | Architecture:<br>00 = Uniform<br>01 = Bottom<br>11 = Top | |

# Conclusion

Contrasting the key differences between Micron's N25Q128_3V parameter blocks and uniform subsector erase serial NOR Flash memory devices enables users to migrate applications smoothly from the parameter blocks device to the uniform subsector erase device. Contact your local representative for additional information.

# Revision History

## Rev. B – 6/11

- Updated nomenclature

## Rev. A – 5/11

- Initial release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
www.micron.com/productsupport Customer Comment Line: 800-932-4992