



# AN309016

## Application note

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### How to Power On and Power Off the Numonyx™ Axcell™ M29F Flash Memory Device

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#### Introduction

This application note describes guidelines on how to provide power supply to and remove power supply from the Numonyx™ Axcell™ M29F flash memory device.

Special attention is given to the required current for the power-on phase, and to the operations a system designer must perform to recover the flash memory if power loss occurs during a modify operation on the memory's main array.

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# 1 Power overview

External power supplies provide memory devices with the electrical current necessary for their internal and external operations.

When implementing power supply solutions, designers have to know the total power required by external supplies (also referred to as “rail power”). Furthermore, designers have to consider how much of the required total power dissipates inside the device (referred to as “thermal power” or “dissipated power”). This is compared to the portion of the total power that dissipates outside the device, such as in external output capacitive loads or balanced resistor termination networks.

The total power used by a device, the output loading, and external termination networks (if any) includes the following major components:

- standby power
- dynamic power
- I/O power

Standby power comes from the  $I_{CC2}$  current circulating within the device when it is in standby mode.

Core dynamic power comes from the internal switching within the device (such as charging and discharging capacitance on internal nodes).

I/O power comes from the external switching of I/O drivers (such as charging and discharging external load capacitance connected to device pins).

The thermal power is the component of total power that dissipates in the device’s package, while the remainder dissipates externally.

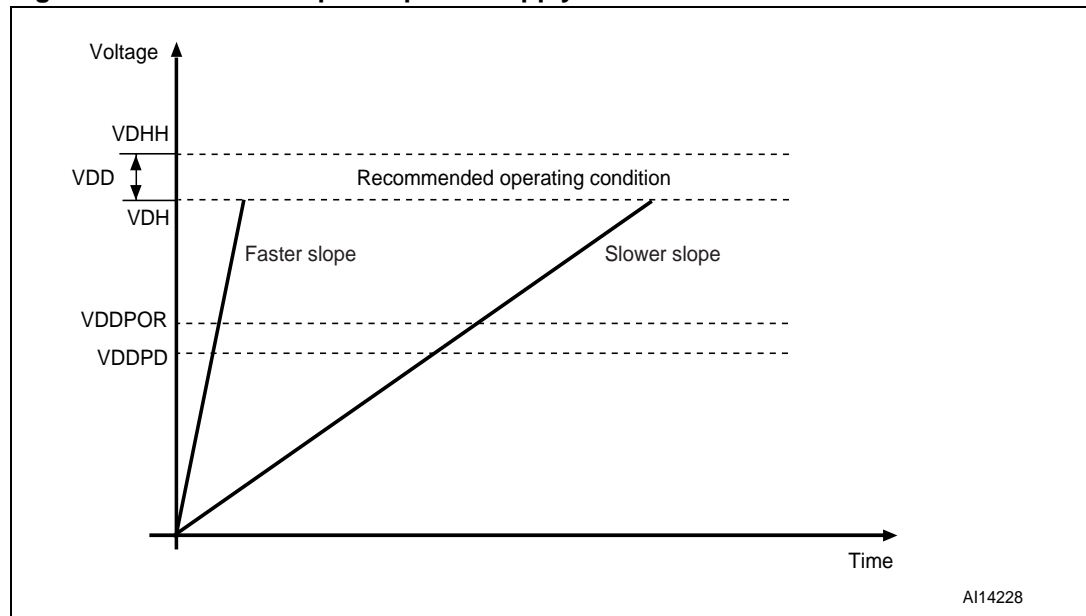
Designers must take into account the thermal power dissipated in the device to understand if the device’s intrinsic heat transfer ability (referred to as “thermal resistance”) is sufficient to keep internal die-junction temperatures within the normal operating specifications. If the device’s thermal resistance is insufficient, additional thermal solutions, such as aluminium heat sinks, can be used to improve heat transfer performance.

Designers must also be aware of the inrush current, which is the total current required by the device to power itself (see [Chapter 2: Inrush current](#)).

## 2 Inrush current

The inrush current is the current required by the device during power-up. During power-up, the device requires a minimum level of current over a specific period of time. The length of this period of time depends on the slope of the power supply while this slope is set to  $I_{CC1}$ ; that is, the the slope is set to the Read current defined in the datasheet (see [Figure 1: Different slopes of power supply](#)).

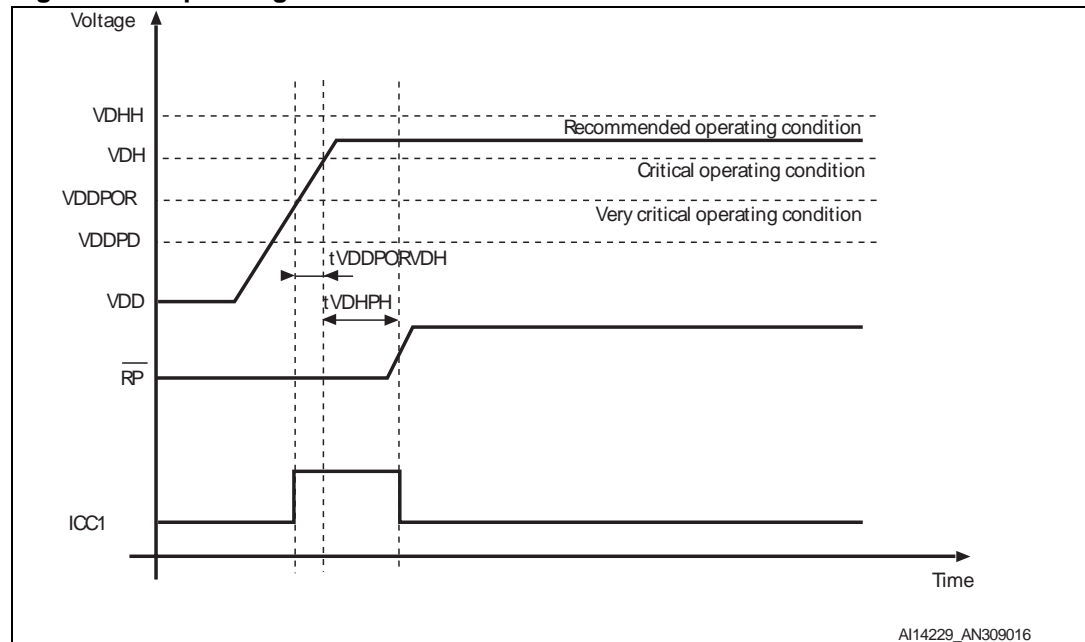
**Figure 1. Different slopes of power supply**



1. The recommended operating condition is the range of power supply in which the memory device is designed to work properly.

When the voltage reaches ninety percent of its nominal value ( $V_{DH} = V_{DD} \text{ min} = 4.5 \text{ V}$  for the Axcell M29F device), the system can de-assert the Reset pin of the memory after a certain time,  $t_{VDHPH}$ . From this time on, the inrush current is no longer dissipated (see [Figure 2: Operating conditions](#)).

Figure 2. Operating conditions

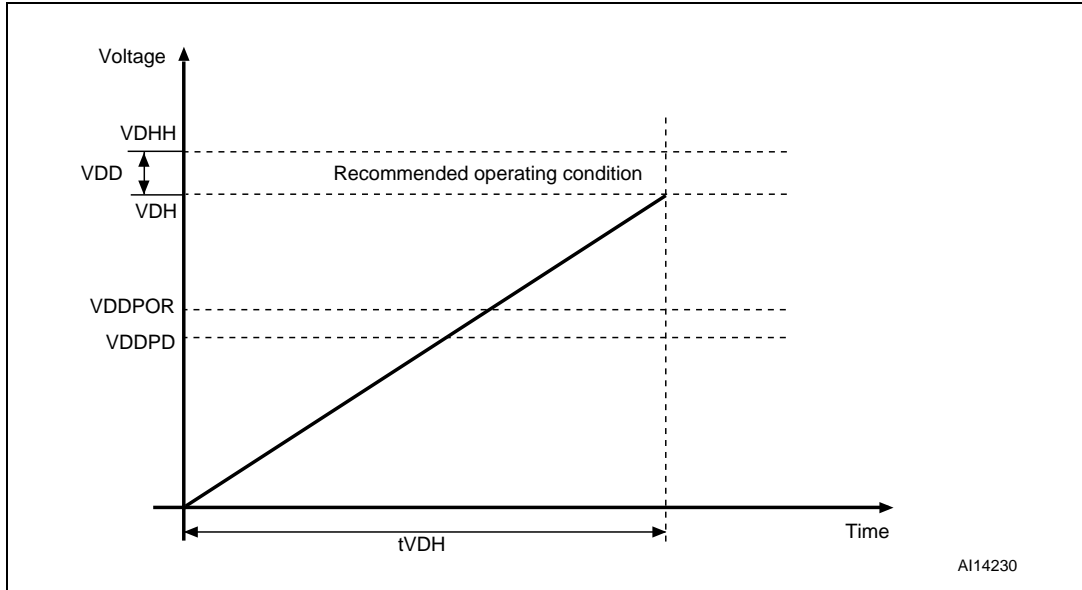


1. The recommended operating condition is the range of power supply in which the memory device is designed to work properly.
2. The critical operating condition is the range of power supply in which the device is not designed to work properly. In this power supply range, the device works with reduced performance but without internal damages.
3. The very critical operating condition is the range of power supply in which the device is not designed to work properly. In this power supply range, only the standby status is guaranteed.

To efficiently charge the board capacitance when the power is first applied, power supplies are commonly designed to provide more current instantaneously than they are rated for, in terms of continuous output. For the majority of designs, the chosen power source is able to provide the required  $I_{CC1}$  without requiring additional components.

To guarantee the power-on of memory devices, the  $V_{DD}$  ramp time,  $t_{VDH}$ , must be no slower than 50 ms during power-on (see [Figure 3: Time to ramp up the VDD power supply](#)). This limitation refers to the slowest ramp time for which the power-on current is formally characterized and tested.  $t_{VDH}$  is measured with a load connected to the power supply.

Figure 3. Time to ramp up the  $V_{DD}$  power supply

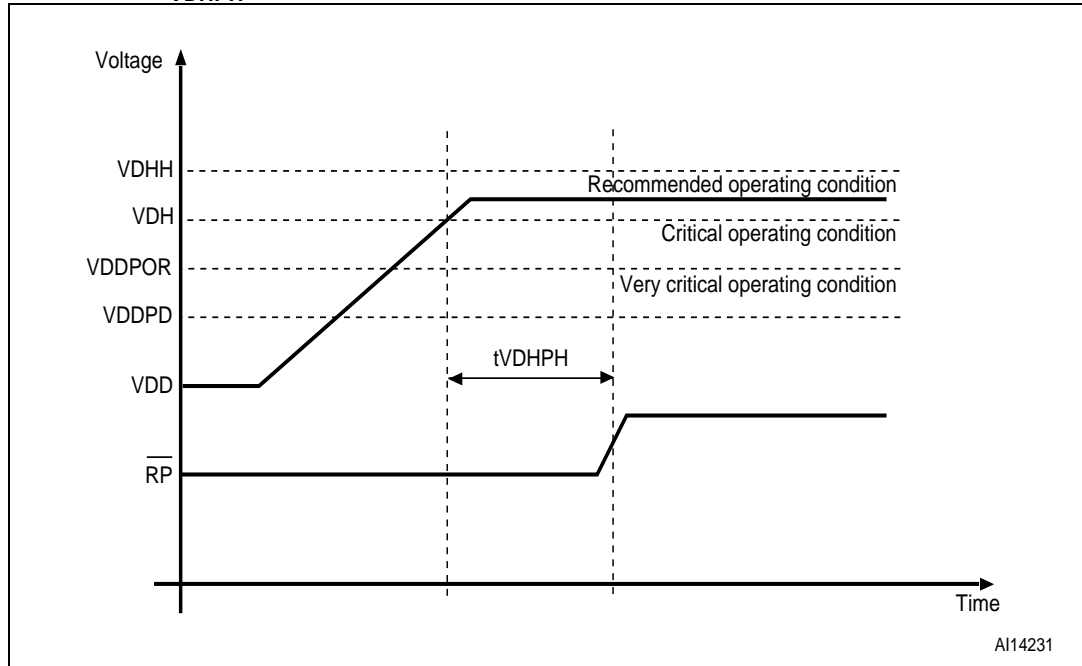


As long as the ramp time is inside the slope limit allowed for power supply, the  $I_{CC1}$  specification does not change. Even though  $V_{DD}$  ramps up quickly, as long as the  $I_{CC1}$  specification is met, the memory device powers on successfully.

### 3 Board power consideration

To avoid any spurious operations inside the memory device during the power-on phase, the Reset pin must be kept Low,  $V_{IL}$ , for a certain period of time,  $t_{VDHPH}$ , as shown in [Figure 4](#). The Reset pin Low maintains the memory in the reset state until the device reaches the recommended operating condition.

**Figure 4.**  $t_{VDHPH}$  definition



## 4 Critical power conditions

The memory works in critical operating conditions when its power supply drops into the voltage range between the  $V_{DDPOR}$  and  $V_{DH}$  values (see [Figure 5: VDD in critical operating conditions](#)). In critical operating conditions, there is no damage to the device, which does not need to be reset.

When the power supply drops below  $V_{DDPOR}$  while remaining above the  $V_{DDPD}$  value, the memory works in critical operating conditions (see [Figure 6: VDD in very critical operating conditions](#)). In very critical operating conditions, the memory keeps working well but its operation is not fully guaranteed because noise on the power supply can bring  $V_{DD}$  below the  $V_{DDPD}$  value.

When the power supply drops below the  $V_{DDPD}$  threshold, the Reset pin of the flash memory must be kept Low,  $V_{IL}$ , until the power supply comes back to the recommended operating conditions (see [Figure 7: VDD below very critical operating conditions](#)).

**Figure 5.  $V_{DD}$  in critical operating conditions**

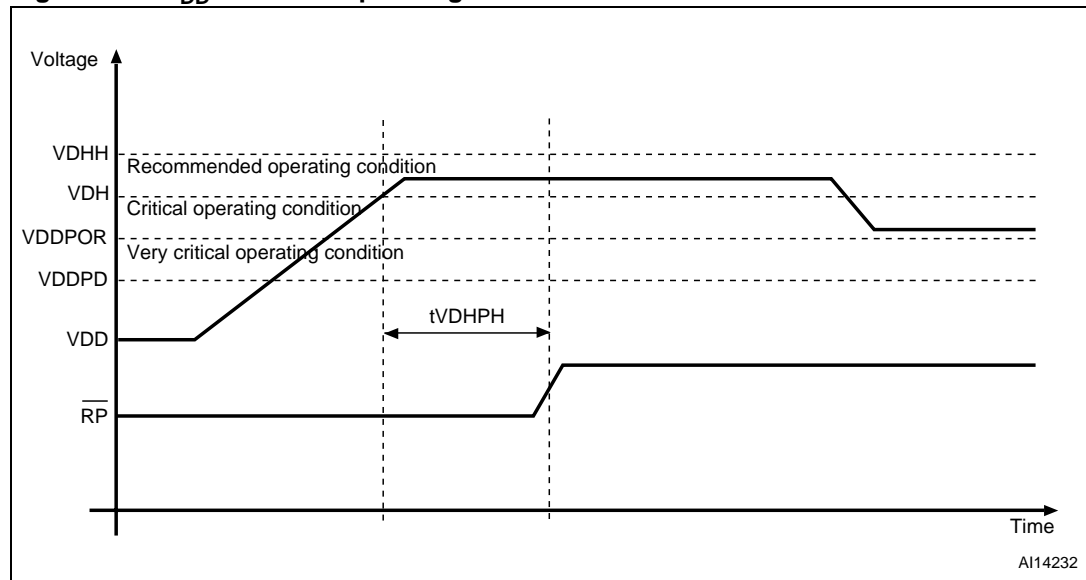


Figure 6.  $V_{DD}$  in very critical operating conditions

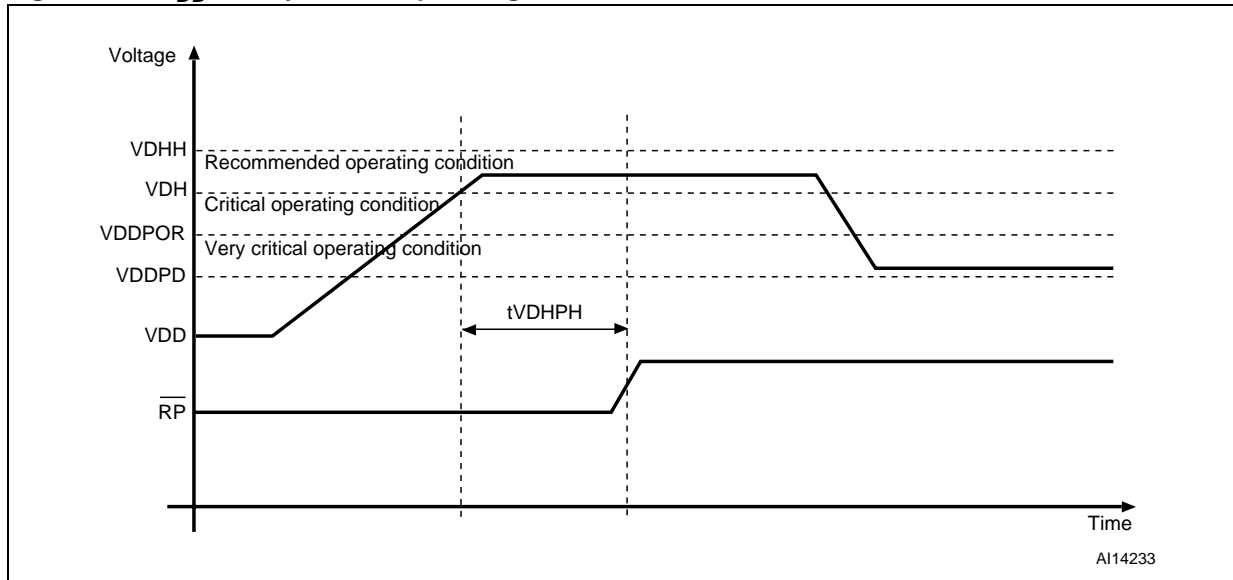
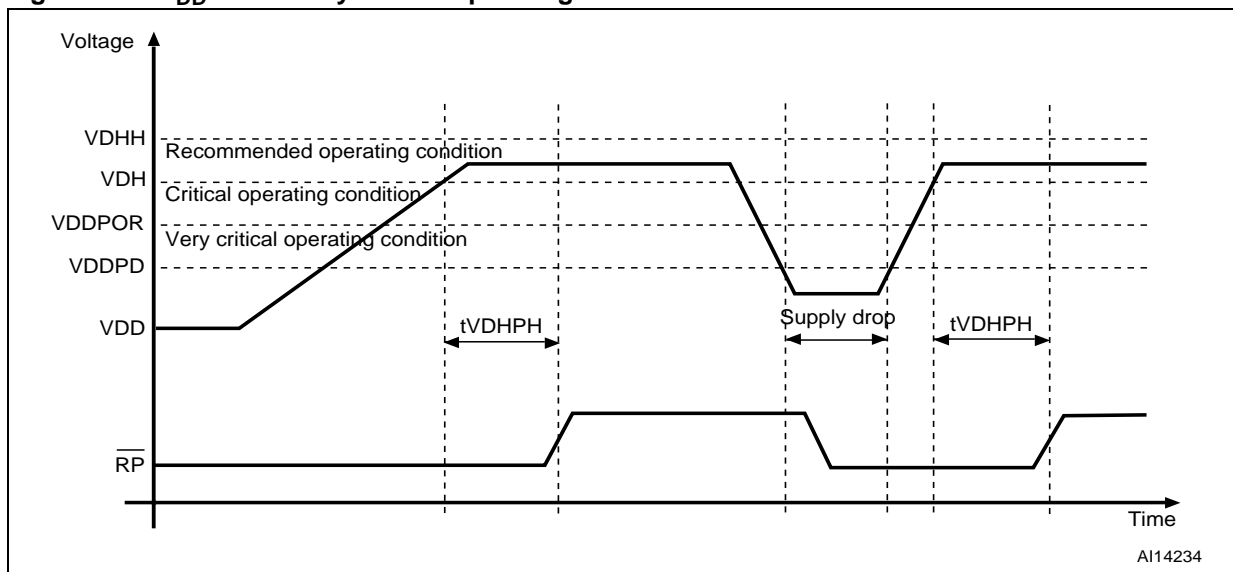


Figure 7.  $V_{DD}$  below very critical operating conditions



## 5 Recovery operations after a power drop

Modify operations in flash memory devices take a long time when compared to the average time required by system operations.

During a modify operation, a drop in the memory's power supply is possible. In this situation a system designer must know how to recover the memory's status by using the recovery operations shown in [Table 1: Recovery operations](#) (please refer to the datasheet for commands not listed).

**Table 1. Recovery operations**

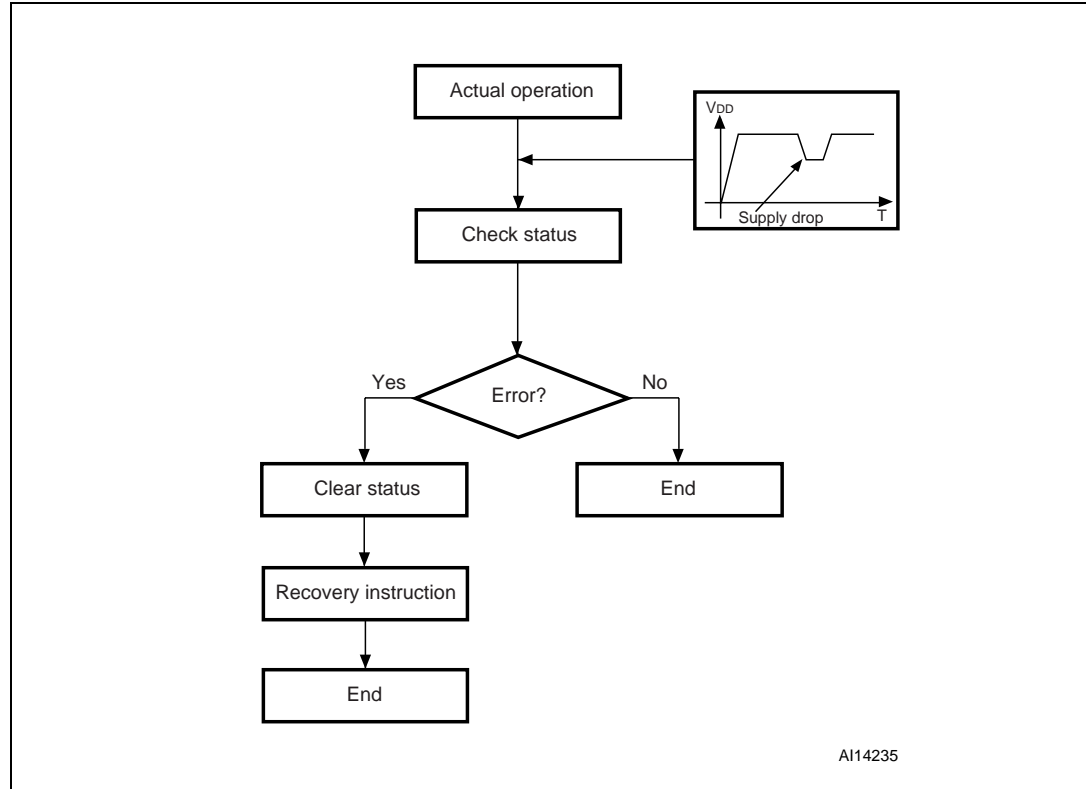
Before the power drop	To recover
<b>Read operations</b>	
Read Array, Read Electronic Signature, Read Status Register, Read Query	Recovery depends upon the previous status of the flash memory. If the status is in modify, please refer to the modify operation section below.
Clear Status Register	Recovery depends upon the previous status of the flash memory. If the status is in modify, please refer to the modify operation section below.
<b>Modify operations</b>	
Chip/Block Erase	Perform a Chip/Block Erase.
Program Suspend	Program (same address, same data)
Erase Suspend	Erase (same block)
Program Resume	Program (same address, same data)
Erase Resume	Erase (same block)
<b>Unlock Bypass operations</b>	
Unlock Bypass/ Unlock Bypass Reset	No specific recovery instruction is required
Unlock Bypass Program/	Perform the same command(Same address, sameblock) following the right flow to issue it

If the power loss is not intense enough to trigger the power-down of the memory device, the ongoing flash operation can be corrupted. In this case, the system designer must check the memory's Status Register to understand if the flash memory device needs to be recovered or not.

The system designer chooses whether to clear the memory's Status Register or not. If the designer chooses to not clear the Status Register, he must know that the information stored in the Status Register is in line with the internal fail status of the flash memory.

The suggested recovery flow is shown in [Figure 8: Recovery flow](#).

Figure 8. Recovery flow



## 6 Glossary

**Table 2. Glossary**

Symbol	Description
$I_{CC2}$	Standby current when the chip is not selected
$I_{CC1}$	Current required to perform the power-on sequence correctly (required Read current)
$V_{DH}$	Minimum power supply voltage (equal to the $V_{dd}$ min = 4.5 V)
$V_{DHH}$	Maximum power supply voltage (equal to the $V_{dd}$ min = 5.5 V)
$V_{DDPOR}$	Minimum power supply during the ramp-up, when the flash memory begins to load all the internal nodes (minimum VLKO voltage = 1.8 V)
$V_{DDPD}$	Threshold value of power supply during the ramp-down, at which point the device shuts down (maximum VLKO voltage = 2.3 V)
$t_{VDHPH}$	Amount of time required to release the Reset pin after the power supply reaches the $V_{DH}$ value (at least 50us after the power supply reaches $V_{DH}$ )
$t_{VDH}$	Time required from power supply to reach the $V_{DH}$ value (max 50 ms, min. 200 us)
$t_{VDDPORVDH}$	Time required between the power supply reaching the $V_{DDPOR}$ value and its reaching the $V_{DH}$ value (the application designer could calculate this value based on the slope of the power supply)

## 7 Revision history

**Table 3. Document revision history**

Date	Revision	Changes
23-Apr-2009	1	Initial release.

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