



# Migration Guide Intel<sup>®</sup> W18-130/90 nm to ST<sup>®</sup> WR-65 nm

Application Note 907

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*September 2008*

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## Revision History

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Date	Revision	Description
July 2008	001	Initial release.

## 1.0 Introduction

This application note describes migrating from the Intel Wireless Flash Memory (W18 130 nm and 90 nm) device to the ST™ Wireless Flash Memory (WR 65 nm) device.

*Note:* For the sake of brevity, throughout the rest of this document, the Intel™ Wireless Flash Memory (W18 90 nm) device is referred to as W18-90 nm, while the Intel™ Wireless Flash Memory (W18 130 nm) device is referred to as W18-130 nm. The ST™ Wireless Flash Memory (WR) 65 nm device is referred to as WR-65 nm.

This document was written based on device information available at the time. Changes in specifications to either device might not be reflected in this document. Refer to the appropriate documents or sales personnel for the current product information before finalizing any design.

**Table 1: Devices to be migrated from Intel W18 (130 nm / 90 nm) to ST WR 65 nm**

Density	Intel W18-130 nm	Intel W18-90 nm	ST WR-65 nm
16 Mbit	N/A	N/A	M58WR016KT M58WR016KB
32 Mbit	XXXXX20XXW0YTQ0 XXXXX20XXW0YBQ0	XXXXX20XXW0YTQE XXXXX20XXW0YBQE	M58WR032KT M58WR032KB
64 Mbit	XXXXX30XXW0YTQ0 XXXXX30XXW0YBQ0	XXXXX30XXW0YTQE XXXXX30XXW0YBQE	M58WR064KT M58WR064KB
128 Mbit	XXXXX40XXW0YTQ0 XXXXX40XXW0YBQ0	N/A	N/A

## 2.0 Package and Ballouts

### 2.1 W18 (130nm/90 nm) to WR (65 nm) 56-Ball Very-thin Fine-pitch Ball Grid Array (VF BGA) Ballout Package Comparison

The WR-65 nm is available in 16-Mbit, 32-Mbit and 64-Mbit densities in the Very-thin Fine-pitch Ball Grid Array (VF BGA) package. This package provides socket compatibility with the W18 (130nm/90nm) in 32-Mbit, 64-Mbit, and 128-Mbit densities only. [Table 2](#) shows the package size and comparison between the W18 product family and the WR product family for a 56- ball VF BGA.

**Table 2: W18 (130nm/90nm) / WR-65 nm Package Size/Ballout Comparison (Sheet 1 of 2)**

Dimension	Symbol	Specification (Dimensions in mm)					
		W18 (130nm/90nm) VF BGA 56 Ball			WR-65 nm VF BGA 56 Ball		
		Min	Nom	Max	Min	Nom	Max
Package Height	A	-	-	1	-	-	1
Ball Height	A1	0.15	-	-	0.2	-	-
Package Body Thickness	A2	-	0.665	-	-	0.66	-

**Table 2: W18 (130nm/90nm) / WR-65 nm Package Size/Ballout Comparison (Sheet 2 of 2)**

Dimension	Symbol	Specification (Dimensions in mm)					
		W18 (130nm/90nm) VFBGA 56 Ball			WR-65 nm VFBGA 56 Ball		
		Min	Nom	Max	Min	Nom	Max
Ball (Lead) Width	b	0.325	0.375	0.425	0.3	0.35	0.4
Package Body Width (all densities excluding 128-Mbit)	D	7.6	7.7	7.8	7.6	7.7	7.8
Package Body Width (128-Mbit 130 nm)	D	10.9	11.0	11.1	N/A	N/A	N/A
Package Body Length	E	8.9	9	9.1	8.9	9	9.1
Pitch	e	-	0.75	-	-	0.75	-
Ball (Lead) Count	N	-	56	-	-	56	-
Seating Plane Coplanarity	Y	-	-	0.1	-	-	0.08
Corner to Ball A1 Distance Along D (all densities excluding 128-Mbit)	S1	1.125	1.225	1.325	-	1.225	-
Corner to Ball A1 Distance Along D (128-Mbit 130 nm)	S1	2.775	2.2875	2.975	N/A	N/A	N/A
Corner to Ball A1 Distance Along E	S2	2.15	2.25	2.35	-	2.25	-

**Figure 1: 56-Ball VF BGA Package Drawing**

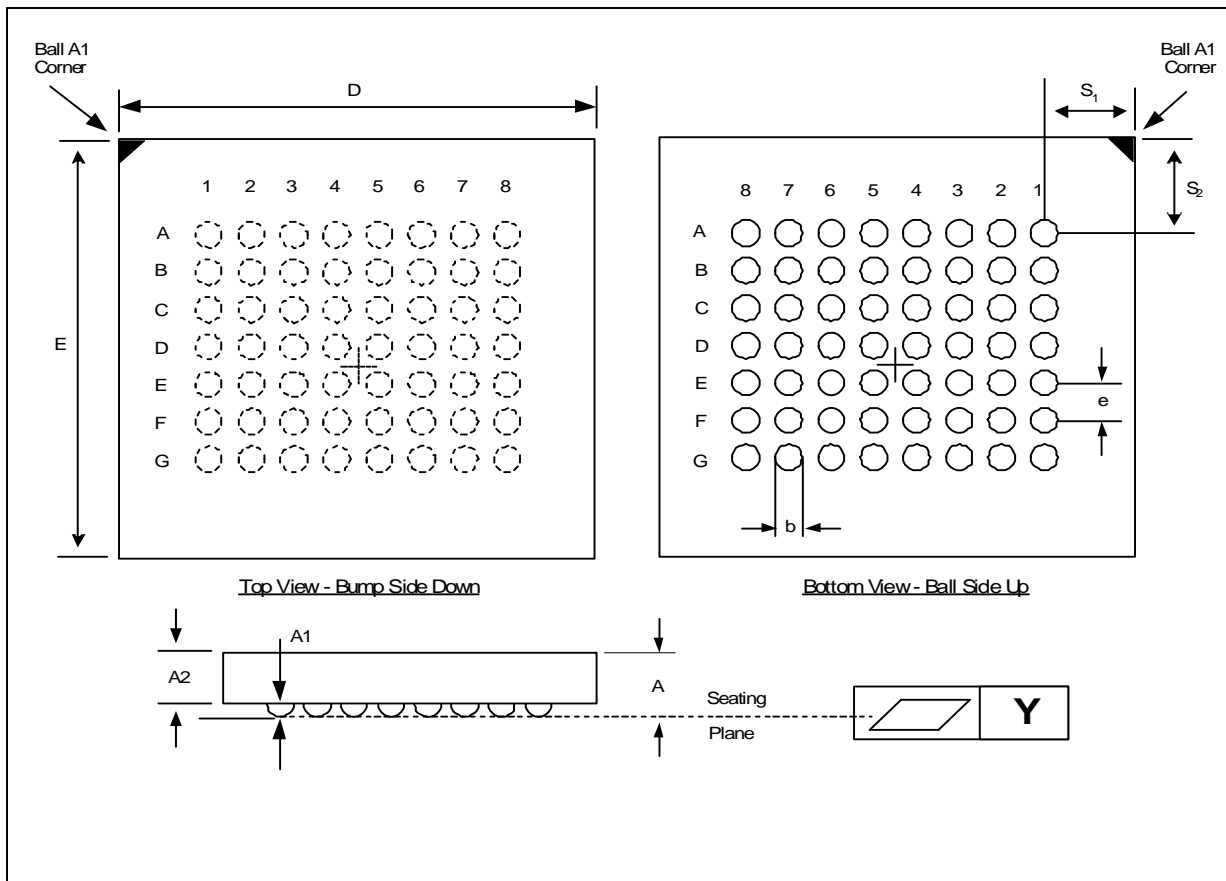
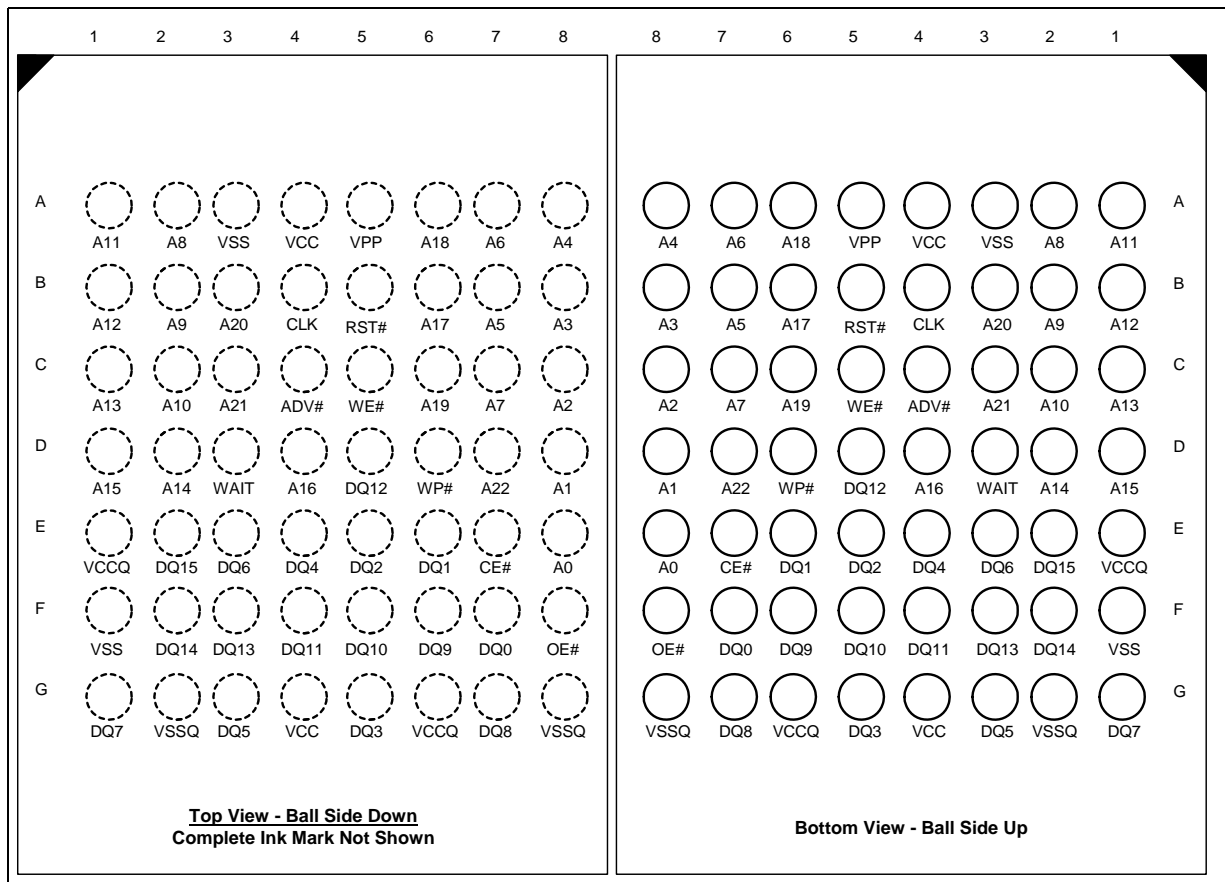


Figure 2: 56-Ball VF BGA Ballout



### 3.0 Manufacturer ID and Device ID

Because each device is manufactured by two different suppliers, the W18 (130nm/90nm) and the ST WR-65 nm have different Manufacturer and Device ID. [Table 3](#) compares the different Manufacturer and Device ID.

**Table 3: Manufacturer ID and Device ID Comparison**

Item	Address		W18 (130nm/90nm)		WR-65 nm	
	Base	Offset	Data	Description	Data	Description
Manufacturer ID	Partition	00h	0089h	Intel	0020h	ST
Device ID	Partition	01h	N/A	N/A	8812h	M58WR016KT 16-Mbit, Top Parameter Device
			N/A	N/A	8813h	M58WR016KB 16-Mbit, Top Parameter Device
			8862h	XXXX20XXW0YTQX 32-Mbit, Top Parameter Device	8814h	M58WR032KT 32-Mbit, Top Parameter Device
			8863h	XXXX20XXW0YBQX 32-Mbit, Bottom Parameter Device	8815h	M58WR032KB 32-Mbit, Bottom Parameter Device
			8864h	XXXX30XXW0YTQX 64-Mbit, Top Parameter Device	8810h	M58WR064KT 64-Mbit, Top Parameter Device
			8865h	XXXX30XXW0YBQX 64-Mbit, Bottom Parameter Device	8811h	M58WR064KB 64-Mbit, Bottom Parameter Device
			8866h	XXXX40XXW0YTQ0 128-Mbit, Top Parameter Device	N/A	N/A
			8867h	XXXX40XXW0YBQ0 128-Mbit, Bottom Parameter Device	N/A	N/A

## 4.0 Max Ratings

The W18 (130nm/90nm) and the ST WR-65 nm have some differences in Max Ratings. The key difference is in the VPP voltage. The max VPP voltage for the W18 (130nm/90nm) is 13.1 V, while the max VPP voltage for the WR-65 nm is 10 V. Max Ratings differences are summarized in [Table 4](#) compares various features and specifications of each device.

**Table 4: Max Ratings Comparisons**

Parameter	Specification			
	W18 (130nm/90nm)		WR-65 nm	
	Min	Max	Min	Max
Vpp Voltage	-0.2 V	13.1 V	-0.2 V	10 V

## 5.0 Operating Conditions

The W18 (130nm/90nm) and the ST WR-65 nm have some differences in Operating Conditions. Note differences in  $V_{CC}$ ,  $V_{CCQ}$ , and  $V_{PP}$ . The key difference is in the  $V_{PP}$  voltage. The max operating  $V_{PP}$  voltage in factory programming setting for W18 (130nm/90nm) is 12.6V, while the max  $V_{PP}$  voltage for the WR-65 nm is 9.5 V. As mentioned in the previous section regarding Maximum Ratings that applying a Voltage higher than 10V on WR-65 nm may damage the part. It is imperative that  $V_{PP}$  settings are configured accordingly when migrating from W18 (130nm/90nm) to WR-65 nm. Operating Conditions differences are summarized in [Table 5](#).

**Table 5: Operating Conditions Comparisons**

Symbol	Parameter	Specification					
		W18-130 nm		W18-90 nm		WR-65 nm	
		Min	Max	Min	Max	Min	Max
$V_{CC}$	V <sub>CC</sub> Supply Voltage	1.7V	1.95	1.7V	1.95V	1.7V	2V
$V_{CCQ}$	I/O Supply Voltage	1.7V	2.24	1.7V	1.95V	1.7V	2V
$V_{PP1}$	$V_{PP}$ Application Programming	0.9V	1.95V	0.9V	1.95V	-0.4V	$V_{DDQ}+0.4V$
$V_{PP2}$	$V_{PP}$ Factory Programming	11.4V	12.6V	11.4V	12.6V	8.5V	9.5V

## 6.0 Electrical Specification

[Table 6](#) compares DC current specification between the W18 (130nm/90nm) and the WR-65 nm.

**Table 6: DC Current Characteristics Comparisons**

Symbol	Parameter	Specification		
			W18 (130nm/90nm)	WR-65 nm
		Test Condition	Max	Max
ICCR	Average VCC Read (Async Page Mode f=13 MHz)	4 Word Read	6 mA	20 mA
	Average VCC Read (Sync CLK = 66 MHz)	Burst length = 4	17 mA	20 mA
		Burst length = 8	20 mA	22 mA
		Burst length = 16	25 mA	27 mA
		Continuous	30 mA	30 mA

## 7.0 AC Characteristics

There are some differences in timing parameters between W18 (130nm/90nm) and WR-65 nm. [Table 9](#) summarizes the Read Operation AC specification between the W18 (130nm/90nm) and the WR-65 nm.

**Table 7: Read Operation AC Characteristics Comparisons (Sheet 1 of 2)**

Symbol	Parameter	Specification					
		W18-130 nm		W18-90 nm		WR-65 nm	
		Min	Max	Min	Max	Min	Max
$t_{AVAV}$	Read Cycle Time	60 ns	-	60 ns	-	70 ns	-
$t_{AVQV}$	Address to Output Valid	-	60 ns	-	60 ns	-	70 ns
$t_{ELQV}$	CE# Low to Output Valid	-	60 ns	-	60 ns	-	70 ns
$t_{PHQV}$	RST# High to Output Valid	-	150 ns	-	150 ns	-	-
$t_{EHQZ}$	CE# High to Output High-Z	-	14 ns	-	14 ns	-	17 ns
$t_{ELTV}$	CE# Low to WAIT Valid	-	11 ns	-	11 ns	-	14 ns
$t_{EHTZ}$	CE# High to WAIT High-Z	-	14 ns	-	11 ns	-	14 ns
<b>Latching Specifications</b>							
$t_{AVVH}$	Address Setup to ADV# High	7 ns	-	7 ns	-	9 ns	-
$t_{VLQV}$	ADV# Low to Output Valid	-	60 ns	-	60 ns	-	70 ns
$t_{VLVH}$	ADV# Pulse Width Low	7 ns	-	7 ns	-	9 ns	-
$t_{VHVL}$	ADV# Pulse Width High	7 ns	-	7 ns	-	-	-

**Table 7: Read Operation AC Characteristics Comparisons (Sheet 2 of 2)**

Symbol	Parameter	Specification					
		W18-130 nm		W18-90 nm		WR-65 nm	
		Min	Max	Min	Max	Min	Max
$t_{VHAX}$	Address Hold from ADV# High	7 ns	-	7 ns	-	9 ns	-
<b>Clock Specifications</b>							
$t_{CH/L}$	CLK High or Low Time	3.5 ns	-	3.5 ns	-	4.5 ns	-
<b>Synchronous Specifications</b>							
$t_{AVCH}$	Address Valid Setup to CLK	7 ns	-	7 ns	-	9 ns	-
$t_{VLCH}$	ADV# Low Setup to CLK	7 ns	-	7 ns	-	9 ns	-
$t_{ELCH}$	CE# Low Setup to CLK	7 ns	-	7 ns	-	9 ns	-
$t_{CHAX}$	Address Hold from CLK	7 ns	-	7 ns	-	9 ns	-

Table 8 summarizes the Write Operation AC specification between the W18 (130nm/90nm) and the WR-65 nm.

**Table 8: Write Operation AC Characteristics Comparisons**

Symbol	Parameter	Specification			
		W18 (130nm/90nm)		WR-65 nm	
		Min	Max	Min	Max
$t_{WLWH}$ ( $t_{ELEH}$ )	WE# (CE#) Write Pulse Width Low	40 ns	-	45 ns	-
$t_{DVWH}$ ( $t_{DVEH}$ )	Data Setup to WE# (CE#) High	40 ns	-	45 ns	-
$t_{AVWH}$ ( $t_{AVEH}$ )	Address Setup to WE# (CE#) High	40 ns	-	45 ns	-
$t_{WHWL}$ ( $t_{EHEL}$ )	WE# (CE#) Pulse Width High	20 ns	-	25 ns	-

## 8.0 Program/Erase Timing Characteristics

**Table 9** summarizes the Program/Erase Timing characteristics between the W18 (130nm/90nm) and the WR-65 nm. On the WR-65 nm a maximum program/erase time does not exist on some specifications. In these cases, the status register must be polled to determine when programming has completed. Additionally, the WR-65 nm family has additional Double Word and Quad Word Factory programming which improve write throughput in factory programming mode. Please refer to the WR-65 nm datasheet (M58WRxxxKT, M58WRxxxKB) for more information regarding Double Word and Quad Word Factory programming.

**Table 9: Program/Erase Timing Characteristics Comparisons**

Operation	Parameter	Description	Specification								
			W18 (130nm/90nm)				WR-65 nm				
			VPP1		VPP2		VPP1		VPP2		
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Erase											
Erase Times	$t_{ERS/PB}$	4-Kword Parameter Block	0.3 s	2.5 s	0.25 s	2.5 s	0.3 s	2.5 s	0.25 s	2.5 s	
	$t_{ERS/MB}$	32-Kword Main Block	0.7 s	4 s	0.4 s	4 s	1 s	4 s	0.8 s	4 s	
Programming											
Program Time	$t_{PROG/W}$	Single Word	12 $\mu$ s	150 $\mu$ s	8 $\mu$ s	130 $\mu$ s	12 $\mu$ s	100 $\mu$ s	10 $\mu$ s	100 $\mu$ s	
	$t_{PROG/PB}$	4-Kword Parameter Block	0.05 s	0.23 s	0.03 s	0.07 s	0.04 s	-	0.04 s	-	
	$t_{PROG/MB}$	32-Kword Main Block	0.4 s	1.8 s	0.24 s	0.6 s	0.3 s	-	0.3 s	-	
Factory Programming											
Program	$t_{EFP/W}$	Single Word/Double Word/ quadruple word	-	-	3.1 $\mu$ s	16 $\mu$ s	-	-	10 $\mu$ s	100 $\mu$ s	
	$t_{EFP/PB}$	4-Kword Parameter Block	Enhanced Factory	-	-	15 ms	-	-	-	45 ms	-
			Quad-Enhanced Factory	-	-	-	-	-	-	11 ms	-
			Quad Word	-	-	-	-	-	-	10 ms	-
	$t_{EFP/MB}$	32-Kword Main Block	Enhanced Factory	-	-	120 ms	-	-	-	360 ms	-
			Quad-Enhanced Factory	-	-	-	-	-	-	94 ms	-
Quad Word			-	-	-	-	-	-	80 ms	-	
Operation Latency	$t_{EFP/SETUP}$	EFP Setup	-	-	-	5 $\mu$ s	-	-	-	-	
	$t_{EFP/TRAN}$	Program to Verify Transition	-	-	2.7 $\mu$ s	5.6 $\mu$ s	-	-	-	-	
	$t_{EFP/VERIFY}$	Verify	-	-	1.7 $\mu$ s	130 $\mu$ s	-	-	-	-	

## 9.0 Power and Reset Timing Specifications

Table 10 summarizes the difference in Power and Reset Timing between the W18 (130nm/90nm) and the WR-65 nm.

**Table 10: Power and Reset Timing Comparisons**

Symbol	Parameter	Specification			
		W18 (130nm/90nm)		WR-65 nm	
		Min	Max	Min	Max
$t_{PLPH}$	RST# Low to Reset during Read	100 ns	-	50 ns	-
$t_{PLRH}$	RST# Low to Reset during Block Erase	-	20 $\mu$ s	-	20 $\mu$ s
$t_{PLRH}$	RST# Low to Reset during Program	-	10 $\mu$ s	-	10 $\mu$ s
$t_{VCCPH}$	VCC Power Valid to Reset	60 $\mu$ s	-	200 $\mu$ s	-

**Note:** The WR-65nm devices are slower during the power-on phase; the device is ready for the first operation after 200  $\mu$ s. During the migration, the power-on timing ( $t_{VCCPH}$ ) on the application must be increased to 200  $\mu$ s to wake up the device correctly.

## 10.0 Device Capacitance Characteristics

Table 11 summarizes the Device Capacitance characteristics between the W18 (130nm/90nm) and the WR-65 nm.

**Table 11: Device Capacitance Comparisons**

Symbol	Parameter	Condition	Specification			
			W18 (130nm/90nm)		WR-65 nm	
			Typ	Max	Typ	Max
CCE	CE# Input Capacitance	VIN = 0.0 V	10 pF	12 pF	6 pF	8 pF

## 11.0 CFI Table

Table 12 summarizes differences in the CFI table between the W18 (130nm/90nm) and the WR-65 nm.

**Table 12: CFI Table Comparisons**

Offset	Length	Description	W18 (130nm/90nm)		WR-65 nm	
			Hex Code	Value	Hex Code	Value
1Ch	1	V <sub>CC</sub> logic supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	--19	1.9V	--20	2.0V
1Dh	1	V <sub>PP</sub> [programming] supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	--B4	11.4V	--85	8.5V
1Eh	1	V <sub>PP</sub> [programming] supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	--C6	12.6V	--95	9.5V
23h	1	"n" such that maximum word program time-out = 2 <sup>n</sup> times typical	--04	256 $\mu$ s	--03	128 $\mu$ s
25h	1	"n" such that maximum block erase time-out = 2 <sup>n</sup> times typical	--03	8s	--02	4s
46h	1	V <sub>PP</sub> optimum program/erase supply voltage bits 0–3 BCD value in 100 mV bits 4–7 HEX value in volts	--C0	12.0V	--90	9.0V

**Table 12: CFI Table Comparisons**

48h	4	Protection Field 1: Protection Description Bits 0-7 Lower byte of protection register address Bits 8-15 Upper byte of protection register address Bits 16-23 2n bytes in factory pre-programmed region Bits 24-31 2n bytes in user programmable region	--80	80h	--80	80h
49h			--00	00h	--00	00h
4Ah			--03	8 bytes	--03	8 bytes
4Bh			--03	8 bytes	--04	16 bytes

## 12.0 Conclusion

When migrating from the W18 (130nm/90nm) device family to the WR-65 nm family, user need to keep in mind the major differences in:

- Electronic signature code
- Operation conditions and maximum ratings
- Power-On timing
- CFI information
- DC/AC parameters

User may take advantage of Factory Program commands available on WR-65 nm to speed-up factory programming throughput.

Refer to Datasheet 290701 for information regarding the W18 (130nm/90nm) family and datasheet (M58WRxxxKT, M58WRxxxKB) for more detailed information regarding the WR-65 nm device.