

Migrating from a Chip Enable care to a
Chip Enable don't care NAND flash memory

1 Introduction

All NAND flash memories offered by Numonyx have the Chip Enable don't care feature, which allows to share the bus among several memories active at the same time, as Chip Enable transitions during the latency time do not stop read operations.

The purpose of this application note is to highlight the differences between Chip Enable don't care and Chip Enable care devices. It also explains the advantages of Chip Enable don't care NAND flash memories over Chip Enable care devices in applications.

Chip Enable don't care and standard Chip Enable care NAND flash memories differ only by the sequential row read operation which is allowed in Chip Enable care devices only. All other operations are performed in the same way using the same command set.

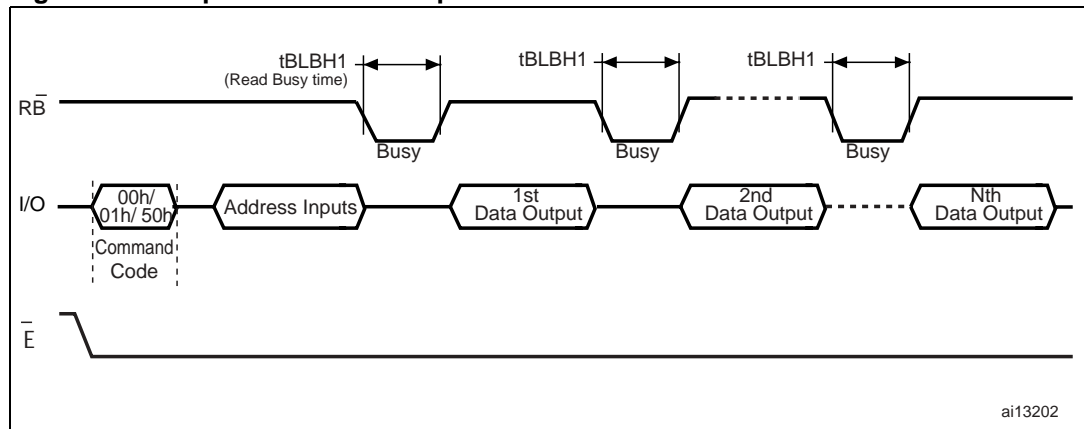
2 Sequential row read in Chip Enable care NAND flash memories

During a read operation in a Chip Enable care NAND flash memory, after the last byte of the page is output, if the Read Enable signal is pulsed and Chip Enable remains Low, then the next page is automatically loaded into the page buffer (see [Figure 1](#)), and the read operation continues.

During sequential row read, the controller issues the Read command only one time at the beginning of the sequence.

A sequential row read operation can only be used to read within a block. If the block changes a new Read command must be issued. A sequential row read operation is terminated by holding the Chip Enable signal High for more than t_{EHEL} .

Figure 1. Sequential row read operation



3 Sequential row read vs random read

Chip Enable don't care NAND flash memories do not feature sequential row read, which means that the Read command has to be issued each time a different page of a block is to be read.

The read time difference, abbreviated RTD, is the difference in time required to read a block using random read (in Chip Enable don't care devices) and sequential row read (in Chip Enable care devices), respectively.

Using sequential row read, the contents of a whole block can be read by issuing only one Read command. The subsequent pages of the same block are automatically loaded into the page buffer when the user reads the last byte of the page.

In Chip Enable don't care NAND flash memories, the maximum RTD value is the additional time required to issue commands and addresses. That is, it is the actual number of write cycles multiplied by t_{WC} , multiplied by the number of pages in the block minus one, which gives:

$$RTD = N_{WC} \times t_{WC} \times (N_P - 1)$$

where:

N_{WC} = number of write cycles (5 = 4 addresses + 1 command for small page devices and 7 = 5 addresses + 2 commands for large page devices)

N_P = number of pages in the block (32 for small page and 64 for large page devices)

The following figures show the read time difference (RTD) for small page and large page NAND flash memories. The RTD is given in μs in [Figure 2](#) and as a percentage in [Figure 3](#). In both figures the cycle time is represented on the X-axis.

[Figure 2](#) shows that to read a whole block in the matrix, the difference between Chip Enable don't care and sequential row read (Chip Enable care) is 0.2-0.3% on nominal cycle time and RTD is less than 3% in the considered worst case (200 ns cycle time).

Figure 2. Read time difference

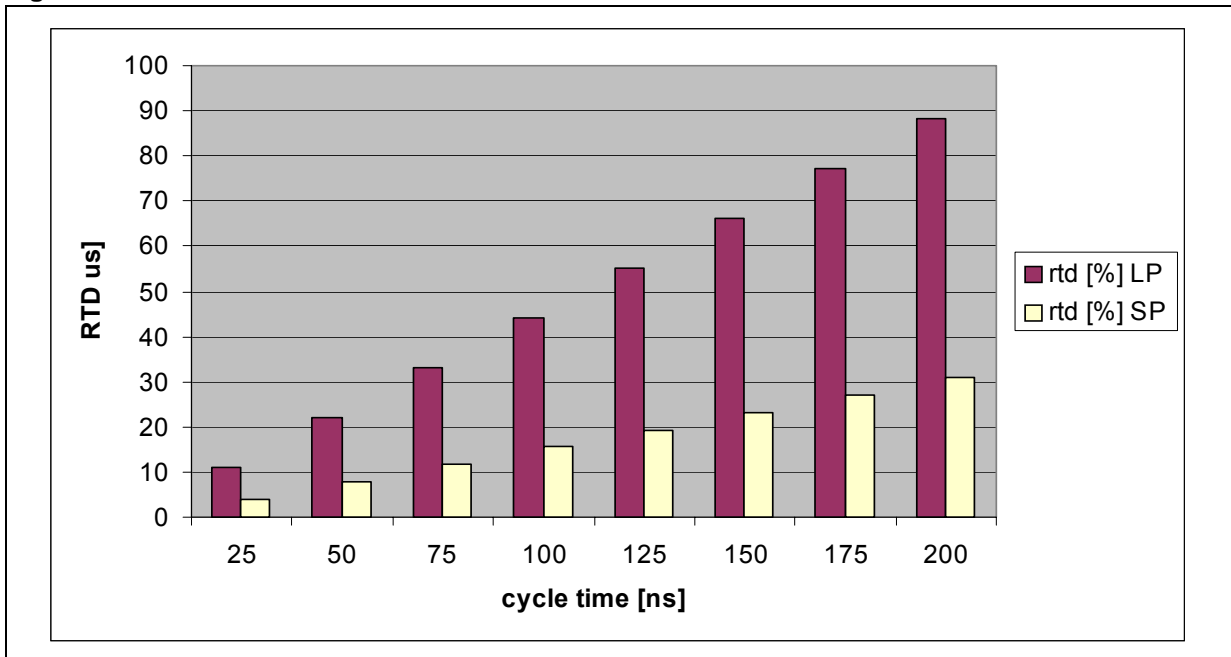
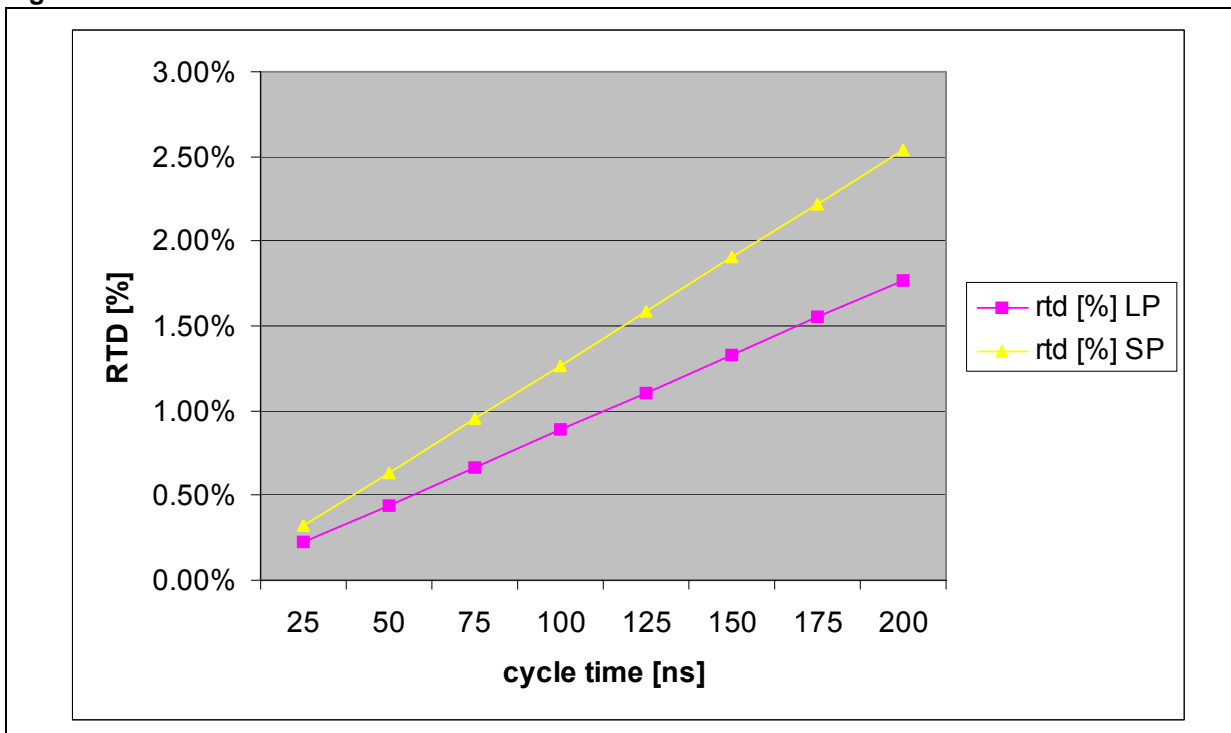


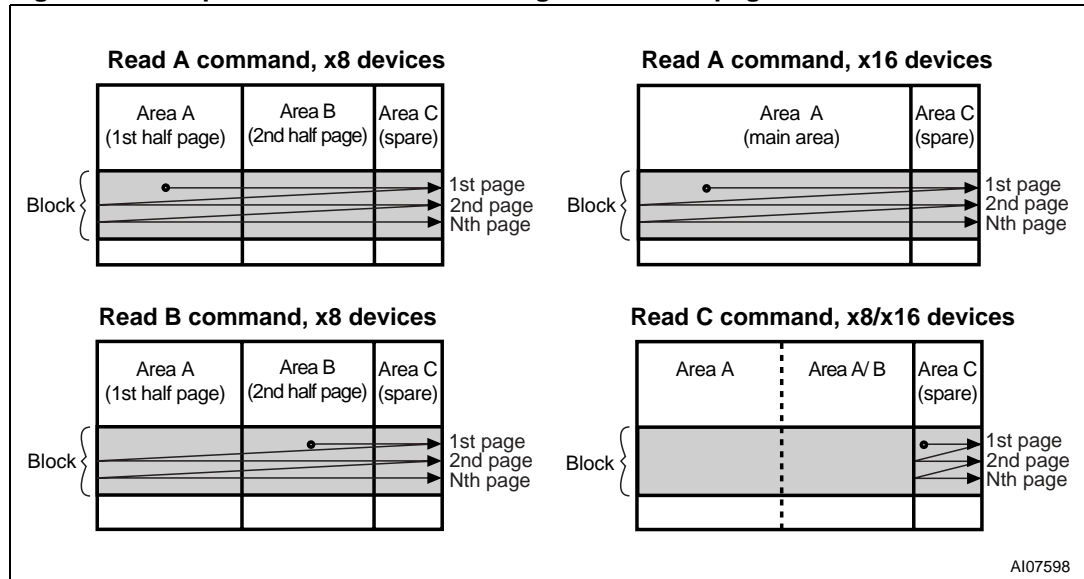
Figure 3. Read time difference vs read time



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Figure 4 shows all the possible applications for sequential row read. The 1st, 2nd ..., Nth pages are read sequentially with no need to issue a Read command between each page. Also, if the first read is performed in the block's spare area, the whole spare area can be read sequentially.

Figure 4. Sequential row read block diagram in small page NAND flash memories



In Chip Enable don't care devices, the array can be scanned exactly as shown in Figure 4, except that the Read command must be issued for each page.

A large number of recent embedded systems are already in line with the Chip Enable don't care specification even if some are still using standard Chip Enable care parts. In fact, issuing the Read command for each page does not affect the NAND flash memory performance. Moreover, the software implementation is easy as it uses loop routines, and the system is more flexible since read is not limited to one block (unlike when using sequential row read in Chip Enable care devices).

5 Conclusions

Numonyx chose to produce Chip Enable don't care NAND flash memories only. The single difference between Chip Enable care and Chip Enable don't care NAND flash memories is the ability of Chip Enable care devices to perform sequential row read operations. The time gained by this additional feature depends on the number of pages to be read and, in all cases, is trivial.

Migrating from a Chip Enable care to a Chip Enable don't care NAND flash memory of the same density, bus width and voltage, may result in a simple plug-and-play operation. For the same density, bus width and voltage, the device code is compatible and the pinout/ballout is identical. Thus, no change is required in the system software and the hardware remains the same provided that it is capable of issuing a Read command for every page read.

6 Revision history

Table 1. Document revision history

Date	Revision	Changes
30-May-2006	1	Initial release.
16-Sep-2008	2	Applied Numonyx branding. Modified Section 3 and Figure 2 . Added Figure 3 .

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