

# Technical Note

## Using Micron® Asynchronous PSRAM with the NXP LPC2292 and LPC2294 Microcontrollers

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### Introduction

The NXP LPC2292 and LPC2294 microcontrollers include an external memory bus that can be used to interface with up to four independently configurable memory devices of 16MB each. This technical note describes the design requirements for a seamless memory connection between this family of NXP microcontrollers and a Micron® asynchronous PSRAM device.

### Micron PSRAM Overview

Micron PSRAM devices are high-speed, CMOS pseudo-SRAM memory devices developed for low-power, portable applications. These devices, which utilize a DRAM-based memory core, are designed to be backward compatible with the more costly 6-transistor asynchronous SRAM and can be used as an SRAM replacement in many applications.

For seamless operation on an SRAM bus, PSRAM products incorporate a transparent self refresh mechanism. This hidden refresh requires no additional support from the system memory controller and has no significant impact on device READ/WRITE performance.

Micron offers both asynchronous and burst PSRAM devices in densities ranging from 8Mb to 128Mb. The 48-ball 70ns asynchronous devices to which this technical note applies are available in 8Mb, 16Mb, 32Mb, or 64Mb densities. The 54-ball 128Mb burst device can also be configured for asynchronous mode operation, but details of that configuration are beyond the scope of this technical note. A future design revision of the 8Mb PSRAM device, slated for production in early 2008, will offer asynchronous READ and WRITE access times of 55ns with a VCC core voltage of 3.3V.

For more information on Micron asynchronous and burst PSRAM devices, refer to the PSRAM parts catalog at [www.micron.com/products/psram/partlist](http://www.micron.com/products/psram/partlist).

### NXP LPC2292/LPC2294 Microcontroller Overview

The LPC2292 and LPC2294 microcontrollers are based on a 16/32-bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, together with 256KB of embedded high-speed Flash memory. The system memory bus is 128 bits wide with 32-bit code execution and up to 60 MHz operation.

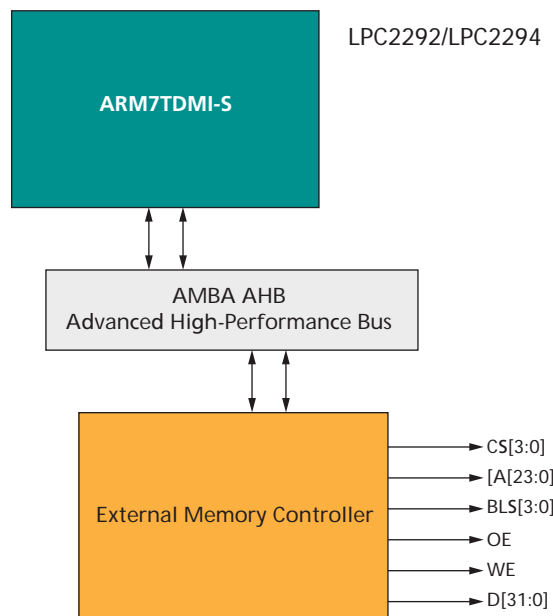
These general-purpose controllers are particularly suitable for automotive and industrial control applications as well as medical systems and fault-tolerant maintenance buses. The LPC2292 has two controller area network (CAN) protocol controllers, and the LPC2294 has four. The CAN protocol is a serial communications protocol with a high level of security. Throughout the rest of this document, "LPC2292" will refer to both the

LPC2292 and the LPC2294 microcontrollers. More information on the NXP LPC2292/LPC2294 family of microcontrollers is available at [www.nxp.com/pip/LPC2292\\_2294\\_5.html](http://www.nxp.com/pip/LPC2292_2294_5.html).

## Memory Interface Description

The external memory controller on the LPC2292 microcontroller is a module that provides an interface between the system bus and external memory devices. It provides support for up to four independently configurable memory banks. Each memory bank is capable of supporting up to 16MB of SRAM, ROM, burst ROM, or NOR Flash memory devices. The external memory data bus can be 8, 16, or 32 bits wide.

Figure 1: External Memory Interface



## PSRAM in Place of SRAM

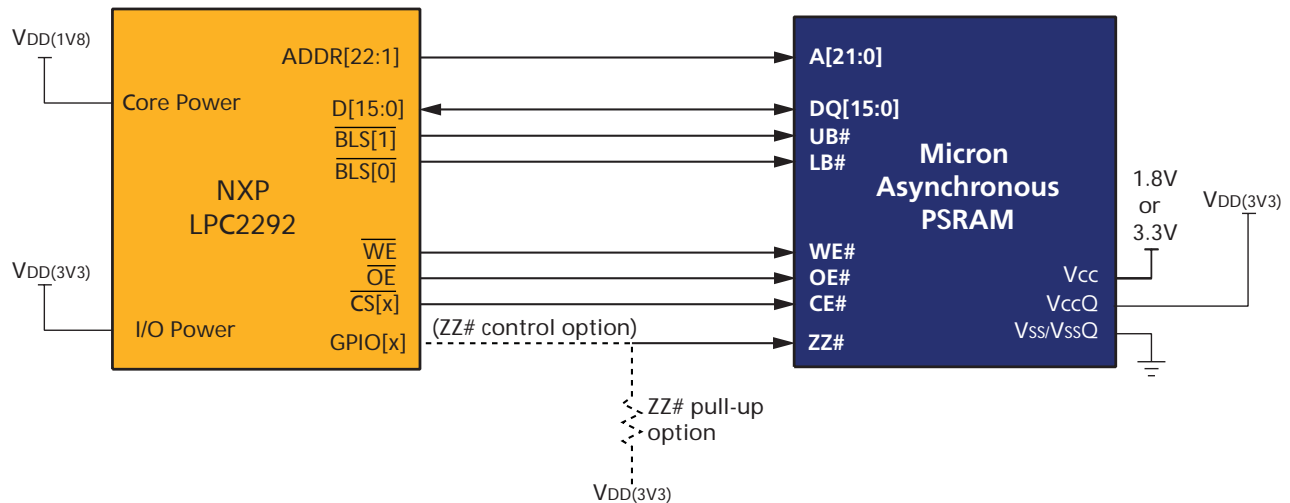
The NXP LPC2292 external memory controller includes four chip selects that can be configured to control up to 16MB (128Mb) of asynchronous memory per chip select. For applications that require SRAM as part of this memory configuration, the Micron 48-ball asynchronous PSRAM device is an effective alternative. Any of the four chip selects can be used to access the PSRAM device unless the system includes an external boot flash that must be connected to CS[0]#. The ZZ# pin of the PSRAM device can be tied HIGH and the device can be left in the default non-page-mode configuration. All other PSRAM signals are connected to the external memory controller precisely as asynchronous SRAM would be connected. Table 1 on page 3 shows all of the signals on the LPC2292 external memory interface and the corresponding 64Mb asynchronous PSRAM signals. Connections for the 8Mb, 16Mb, and 32Mb PSRAM devices are identical except that the higher-order addresses are “no connects.”

Table 1: NXP LPC2292 to PSRAM Pin Assignments

| LPC2292 Signal Name | PSRAM Signal Name | Description                                 |
|---------------------|-------------------|---|
| D[15:0]             | Data [15:0]       | Data  |
| A[22:1]             | A[21:0]           | Address                                     |
| BLS[1]#             | UB#               | Upper byte enable                           |
| BLS[0]#             | LB#               | Lower byte enable                           |
| CS[x]#              | CS#               | Chip select                                 |
| OE#                 | OE#               | Output enable                               |
| WE#                 | WE#               | Write enable                                |
| GPIO[x]             | ZZ#               | Sleep enable, configuration register access |

Figure 2 shows the connections required between the NXP LPC2292 and a 64Mb asynchronous PSRAM device.

Figure 2: NXP LPC2292 to Micron PSRAM Interface



## Deep Power Down

For designs requiring very low standby current, the system designer will need to include control for the PSRAM ZZ# pin via one of the general purpose I/Os available on the LPC2292. This will enable the PSRAM to enter deep power-down (DPD) mode.

## Configuration Register Access

The ZZ# pin is also used to access the configuration register on the PSRAM device. The configuration register defines how the PSRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption in standby mode. The configuration register can also be accessed using a software sequence in cases where the ZZ# pin is not accessible. Further details on accessing the configuration register are contained in the Micron PSRAM data sheets.

## Power Supply Considerations

The NXP LPC2292 microcontroller includes two sets of power supply inputs: VDD(1V8) and VDD(3V3). VDD(1V8) is used to supply internal power to the microcontroller, and VDD(3V3) is used to supply the I/O voltage levels of all external components. The PSRAM device requires a 1.8V VCC core power supply and up to 3.6V supplied to the I/Os through VCCQ. When VDD(3V3) is tied to VCCQ, the processor will match the I/O levels on the PSRAM device.

## LPC2292 Timing Configuration Registers

The VLSI peripheral bus (VPB) divider timing register (VPBDIV[1:0]) on the LPC2292 determines the relationship between the processor clock (CCLK) and the clock used by the external memory controller (XCLK). The maximum processor clock rate is 60 MHz; in order to run the external memory at this frequency, this register must be set to “01b.”

The external memory controller contains four sets of 32-bit registers that control each bank of external memory. These registers must all be set appropriately in order to match the PSRAM 70ns asynchronous timing requirements, which are available in the Micron asynchronous PSRAM data sheets (see “Micron PSRAM Overview” on page 1). Table 2 shows the register setting that would be used for a system with an external memory clock (XCLK) running at the maximum system clock frequency of 60 MHz.

Table 2: NXP LPC2292 Register Settings

| LPC2292 Register | Name     | Description  | Setting |
|------------------|----------|--|---------|
| BCFG0[3:0]       | IDCY     | Number of idle CCLK cycles (+1) between READ and WRITE | 0001    |
| BCFG0[4]         | Reserved | NA   | NA      |
| BCFG0[9:5]       | WST1     | READ access; number of CCLK cycles + 1                 | 00100   |
| BCFG0[10]        | RBLE     | Byte Lines Select (BLS[3:0]) enable during READs       | 1       |
| BCFG0[15:11]     | WST2     | WRITE access; number of CCLK cycles + 1                | 00100   |
| BCFG0[16:23]     | Reserved | N/A  | NA      |
| BCFG0[24]        | BUSERR   | Not used   | 0       |
| BCFG0[25]        | WPERR    | Write protect error                                    | 0       |
| BCFG0[26]        | WP       | Write protect  | 0       |
| BCFG0[27]        | BM       | Burst-ROM  | 0       |
| BCFG0[29:28]     | MW       | Data width; 01 = 16 bit                                | 01      |
| BCFG0[31:30]     | AT       | Not used   | 00      |

## LPC2292 and PSRAM Timing Diagrams

The following timing diagrams compare asynchronous READ and WRITE operations for the LPC2292 microcontroller with the register setting shown in Table 2 on page 4 and for any Micron asynchronous PSRAM devices. The READ register WST1 and WRITE register WST2 are both set to “4” (00100b) in these examples, which corresponds to an access time ( $t_{AA}$  and  $t_{CW}$ ) of 70ns when the system clock is running at 60 MHz.

Figure 3: LPC2292 READ

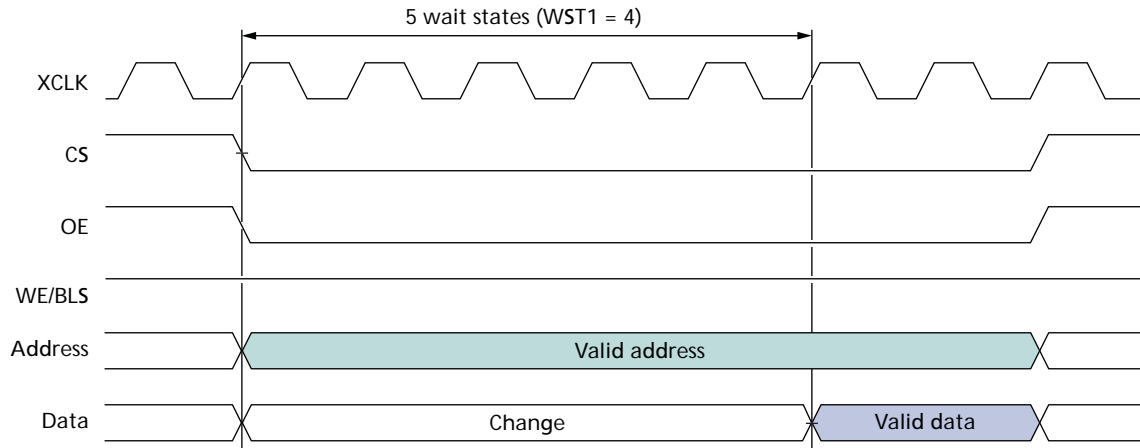


Figure 4: PSRAM READ ( $WE\# = V_{IH}$ )

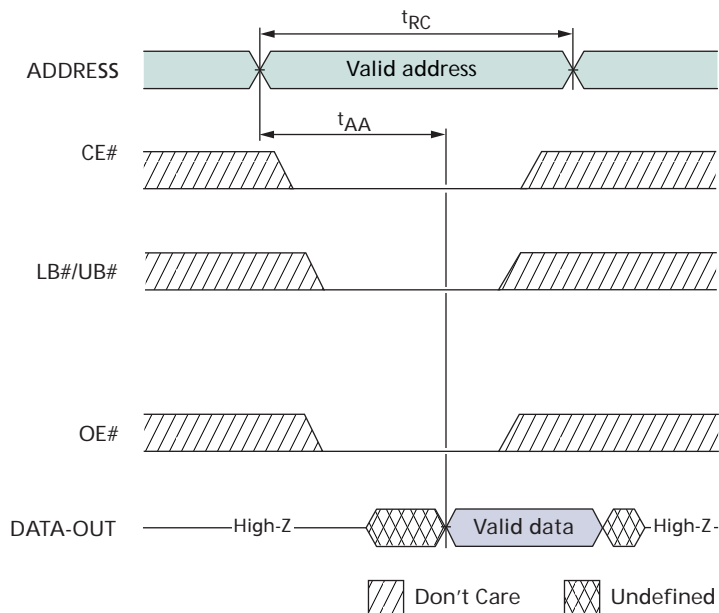


Figure 5: LPC2292 WRITE

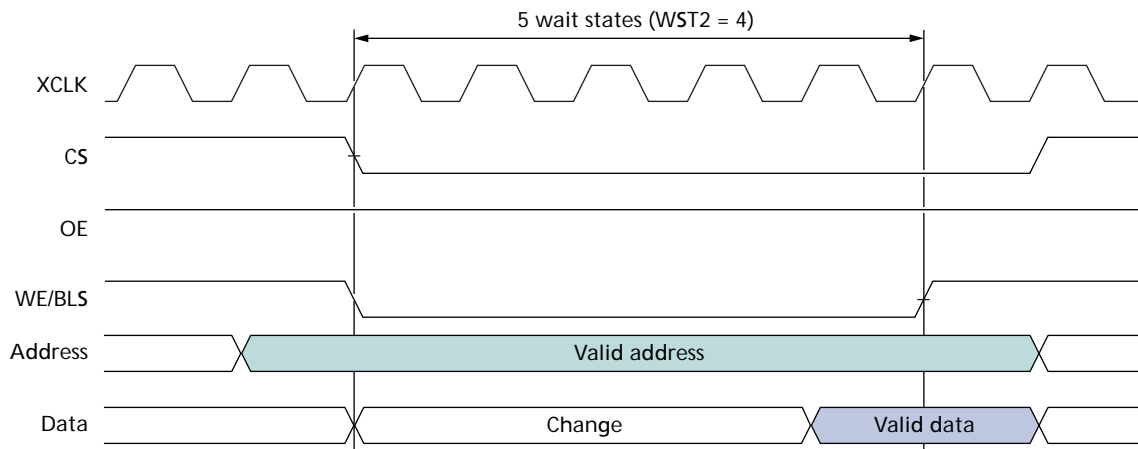
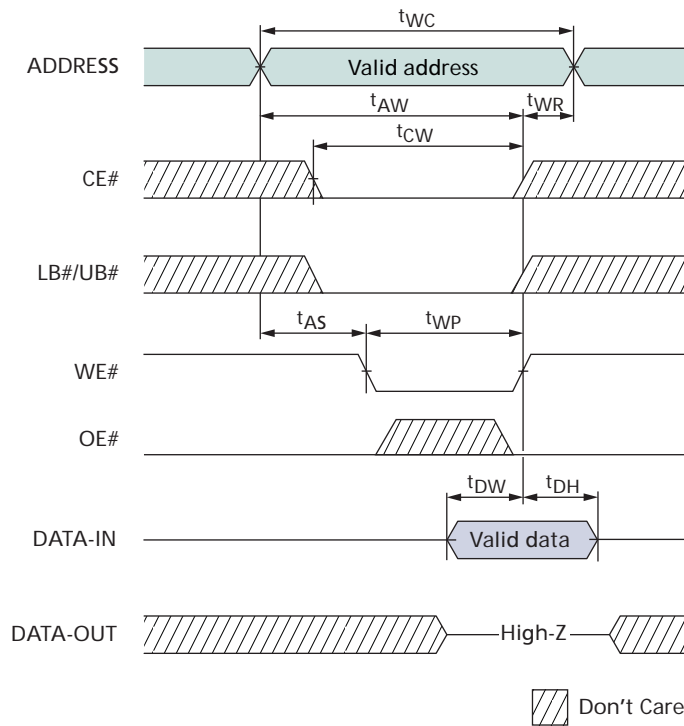


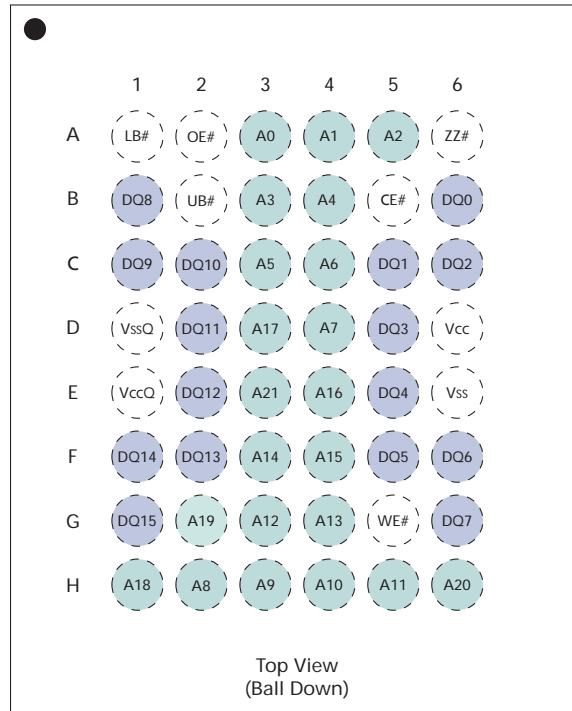
Figure 6: PSRAM WRITE



## PSRAM Package Information

All Micron asynchronous PSRAM devices are available in a 48-ball VFBGA “green” package. The ball assignments for this package are shown in Figure 7.

Figure 7: 48-Ball VFBGA Ball Assignment



## Summary

Micron PSRAM devices offer the benefits of lower cost and seamless integration in place of the more traditional 6-transistor SRAM devices.

This technical note has discussed how to interface any Micron asynchronous PSRAM device with the NXP LPC2292 microcontroller. Specific details regarding timings and register settings are available in the PSRAM data sheet and the LPC2292 data sheet and user's manual (see “References” on page 8).

For any question concerning this information, contact the Micron PSRAM Applications Team at [psramsupport@micron.com](mailto:psramsupport@micron.com).

## References

NXP LPC2292/LPC2294 data sheet:

[www.nxp.com/pip/LPC2292\\_2294\\_5.html](http://www.nxp.com/pip/LPC2292_2294_5.html)

NXP LPC2292/LPC2294 user manual:

Contact your local NXP Semiconductor sales office.

Micron 16Mb asynchronous PSRAM – MT45W1MW16PDGA data sheet:

[www.micron.com/products/psram/partlist](http://www.micron.com/products/psram/partlist)



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