TECHNICAL NOTE

COMPARING MODULE PARAMETERS

Overview

Micron memory modules are continually evolving to higher densities as the components used move to smaller-scale manufacturing processes. A direct consequence of the manufacture of commodity and industry-standard memory modules is that support for previous generations trails off, and the lower-density components are eventually discontinued. The end result is that the number of components required in combination to achieve the higher densities decreases by half.

The customer is often asked to verify support for a reduced chip count module to accomodate this change. This involves aligning the important configurations and parameters with the system controller functionality to ensure compatibility.

Parameters to Compare

The primary parameters that must be compared are:

- Number of ranks on the module (sometimes referred to as module ranks or rows). This determines the number of chip selects necessary for the controller to properly select each rank. Generally, one or two per rank are necessary, depending on the reference design definition.
- Density of each rank. It will either be the total module density for a single-rank module or one-half the total module density for a dual-rank module.
- Row addressing. This is defined by the density of the base device.
- Column addressing. This is defined by both the data width and the density of the base part.
- Refresh rate. This is defined by the density of the base device.
- Module height. Some module configurations are migrating to low-profile (1U-type) support only, and if this could cause a mechanical incompatibility, then it should be considered in your selection.
- Concurrent auto precharge (CAP) support. Industry standards require modules using 256Mb or larger components to support CAP; modules using 128Mb or smaller components are not required to support CAP.

The best way to illustrate this is to give an example of a typical migration to a reduced chip count module.

Figure 1: Comparison Example

Existing Module Solution: MT18LSDT3272DG - Base component: 128Mb, (16 Meg x 8)

- 18-component dual-rank module arranged as 9 components/rank
- 4 chip selects required (2 chip selects per rank)2
- 12 row addresses
- 10 column addresses
- 4K row refresh1
- Does not support CAP (industry-standard definition)

Replacement Module Solution: MT9LSDT3272G - Base component: 256Mb, (32 Meg x 8)

- 9-component single-rank module arranged as 9 components/rank
- 2 chip selects required (2 chip selects per rank)2
- 13 row addresses
- 10 column addresses
- 8K row refresh
- Supports CAP (industry-standard definition)

NOTE:

1. The industry reference design for this module family indicates that to address these parts in x32 segments, two Chip Selects are used per module rank.
2. Addressing may also be annotated as 12/10/4, which is in the format Row/Column/Refresh Rate.

Comparison Chart

When the base component configuration of the module is known (see Module Product Guide), the parameters are compared to the old and new modules for compatibility using the following chart.

Table 1: Module Parameter Comparison

DISCRETE CONFIGURATION	ROW ADDRESSING	COLUMN ADDRESSING	REFRESH COUNT
16M4, 64Mb (x4)	4K (A0-A11) = 12	1K (A0–A9) = 10	4K
8M8, 64Mb (x8)	4K (A0-A11) = 12	512 (A0–A8) = 09	4K
4M16, 64Mb (x16)	4K (A0-A11) = 12	256 (A0–A7) = 08	4K
32M4, 128Mb (x4)	4K (A0-A11) = 12	2K (A0–A9, A11) = 11	4K
16M8, 128Mb (x8)	4K (A0-A11) = 12	1K (A0–A9) = 10	4K
8M16, 128Mb (x16)	4K (A0-A11) = 12	512 (A0–A8) = 09	4K
64M4, 256Mb (x4)	8K (A0-A12) = 13	2K (A0–A9, A11) = 11	8K
32M8, 256Mb (x8)	8K (A0-A12) = 13	1K (A0–A9) = 10	8K
16M16, 256Mb (x16)	8K (A0-A12) = 13	512 (A0–A8) = 09	8K
128M4, 512Mb (x4)	8K (A0-A12) = 13	4K (A0–A9, A11, A12) = 12	8K
64M8, 512Mb (x8)	8K (A0-A12) = 13	2K (A0–A9, A11) = 11	8K
32M16, 512Mb (x16)	8K (A0-A12) = 13	1K (A0–A9) = 10	8K
256M4, 1Gb (x4)	16K (A0-A13) = 14	4K (A0–A9, A11, A12) = 12	8K
128M8, 1Gb (x8)	16K (A0-A13) = 14	2K (A0–A9, A11) = 11	8K
64M16, 1Gb (x16)	16K (A0-A13) = 14	1K(A0–A9) = 10	8K

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