400 MT/s NAND Interface Solutions

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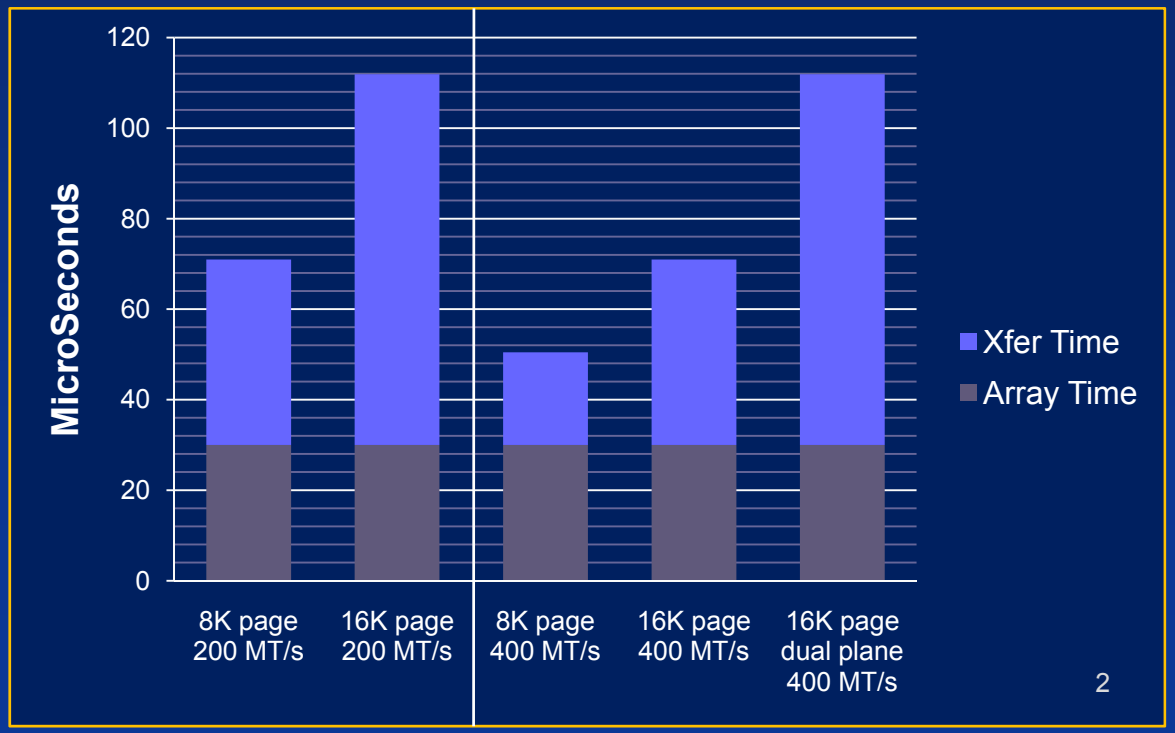
Why 400 MT/s Interface Speeds?

- NAND architectures are moving toward larger data transfer sizes
- Increased bandwidth
  - High-performance computing applications
    - High-density SSDs
    - USB 3.0
- Reduced latency



400 MT/s NAND Interface Solutions

- ONFI 3.0 NV-DDR2
  - Released March 2011
  - ONFI 3.0 Webinar: micron.com/ONFI-3
- Toggle Mode 2.0
  - Announced July 2010
- Work occurring in JEDEC on 400 MT/s
- Reduced CIO
  - Removes features to reduce loading

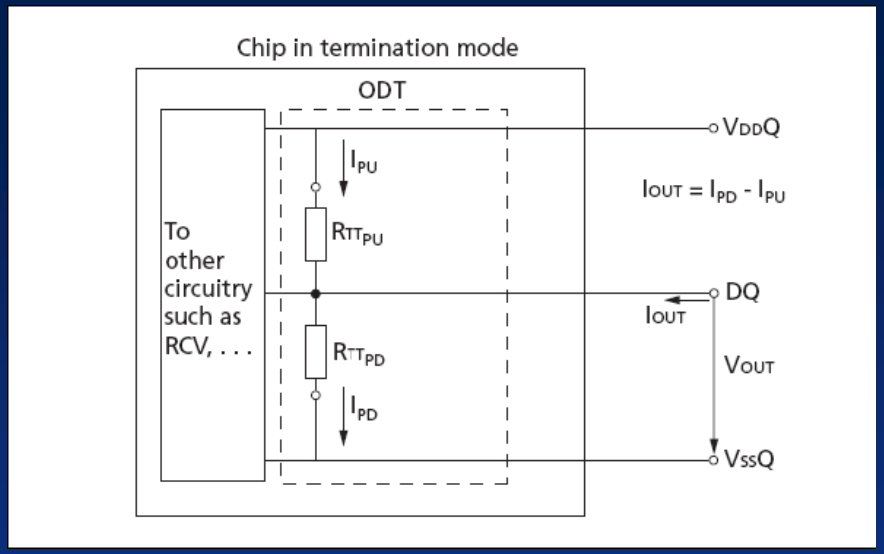
Toggle Mode 2.0

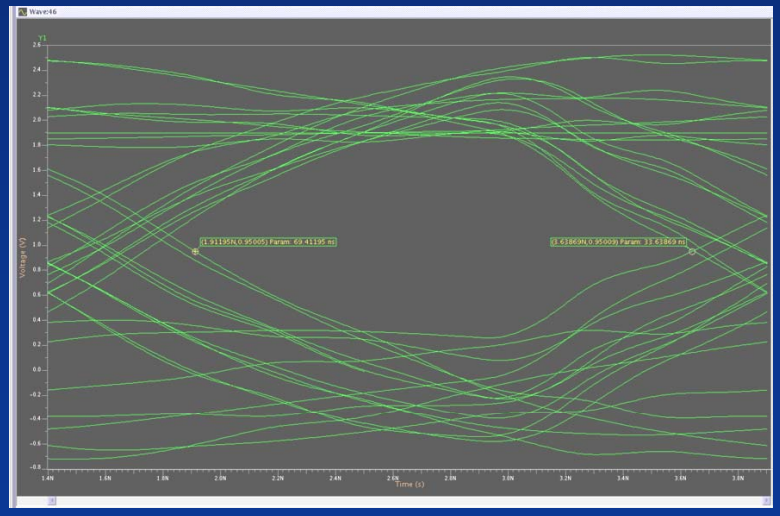
- 400 MT/s DDR interface
  - Compatible with ONFI 3.0 NV-DDR2
- Differential signaling (RE and DQS)
- On-die termination
- External V_{REFQ}
- Reduced signaling (SSTL_18)
- Warm-up cycles

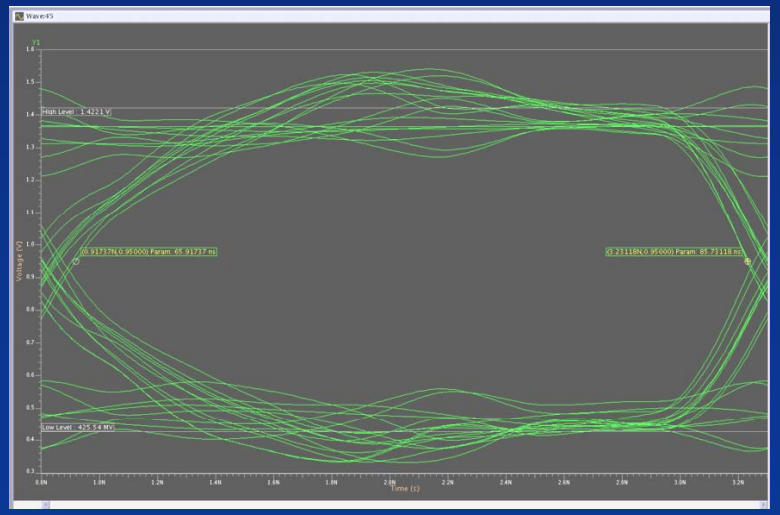
ONFI 3.0 NV-DDR2

- 400 MT/s DDR interface
  - Superset of Toggle Mode 2.0
- Differential signaling (RE and DQS)
- On-die termination
- External V_{REFQ}
- Reduced signaling (SSTL_18)
- Warm-up cycles
- Matrix on-die termination
- Volume addressing

Benefits of Termination







Power Costs of Termination

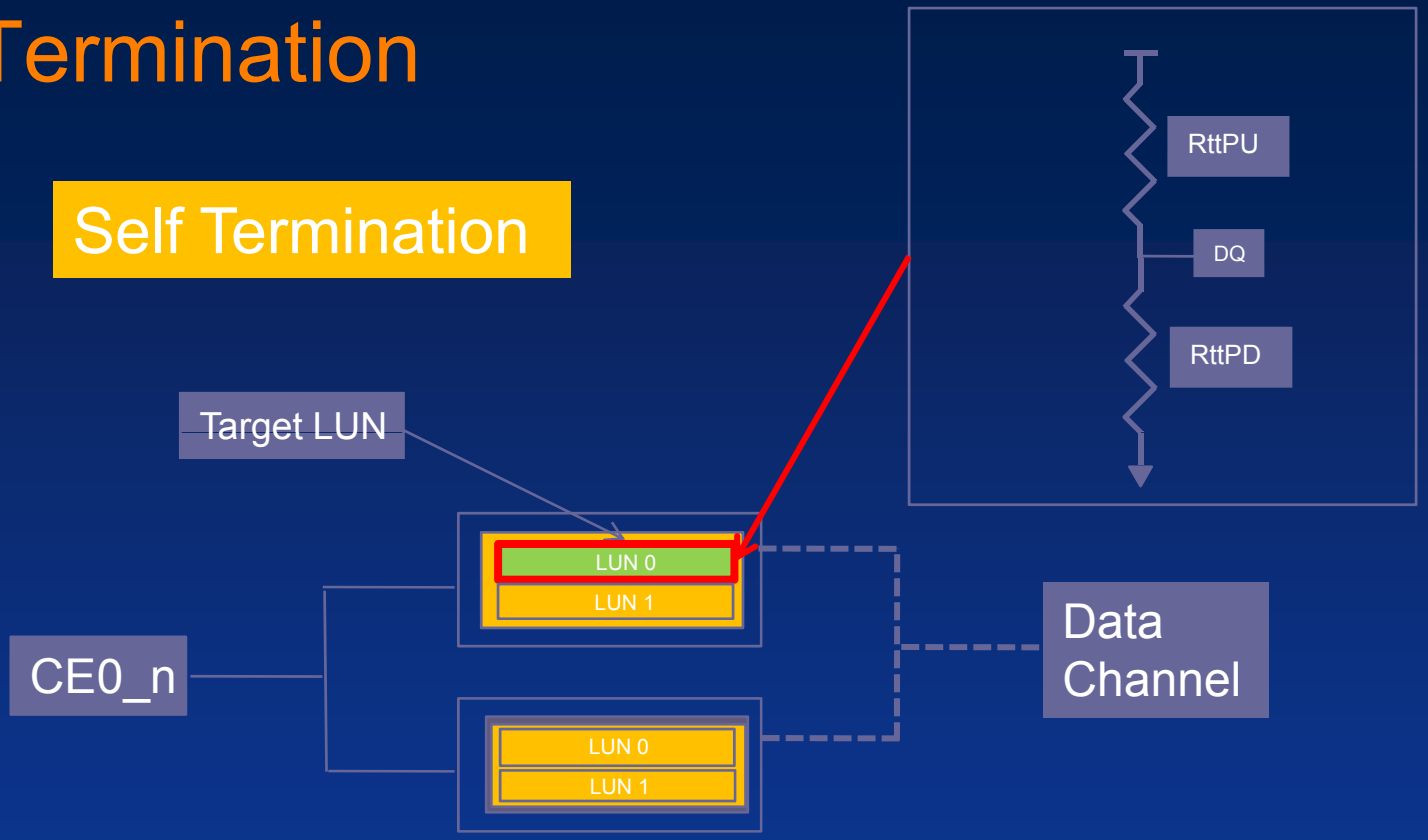
To achieve R_{TT} of 50 ohms:

R_{TTPU} = 100 ohms
R_{TTPD} = 100 ohms

With 1.8V V_{CCQ}, each DQ draws ~9mA

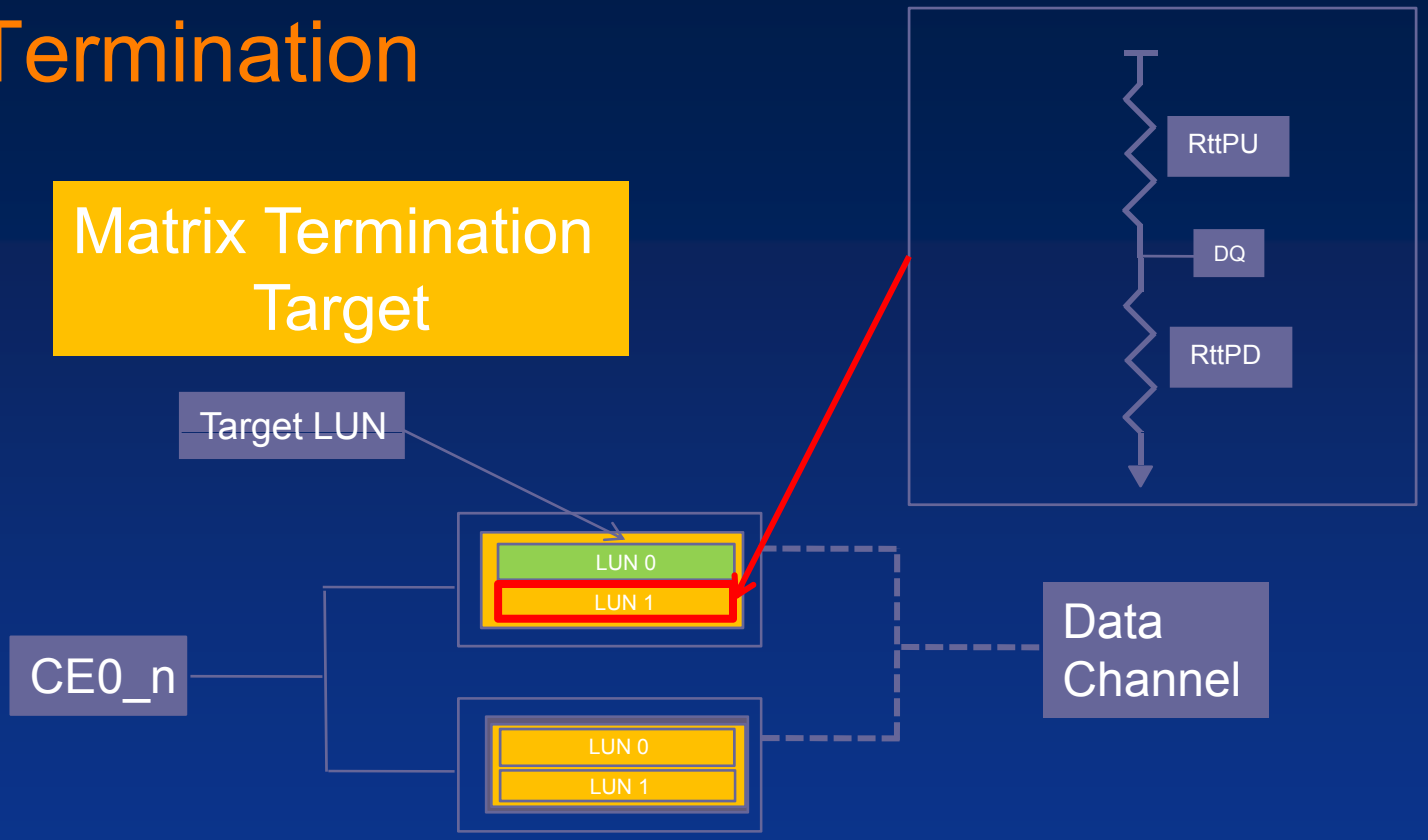
For all terminated signals, this amounts to ~160mW per channel to achieve 50 ohms termination with linear termination

Matrix Termination vs. Self Termination



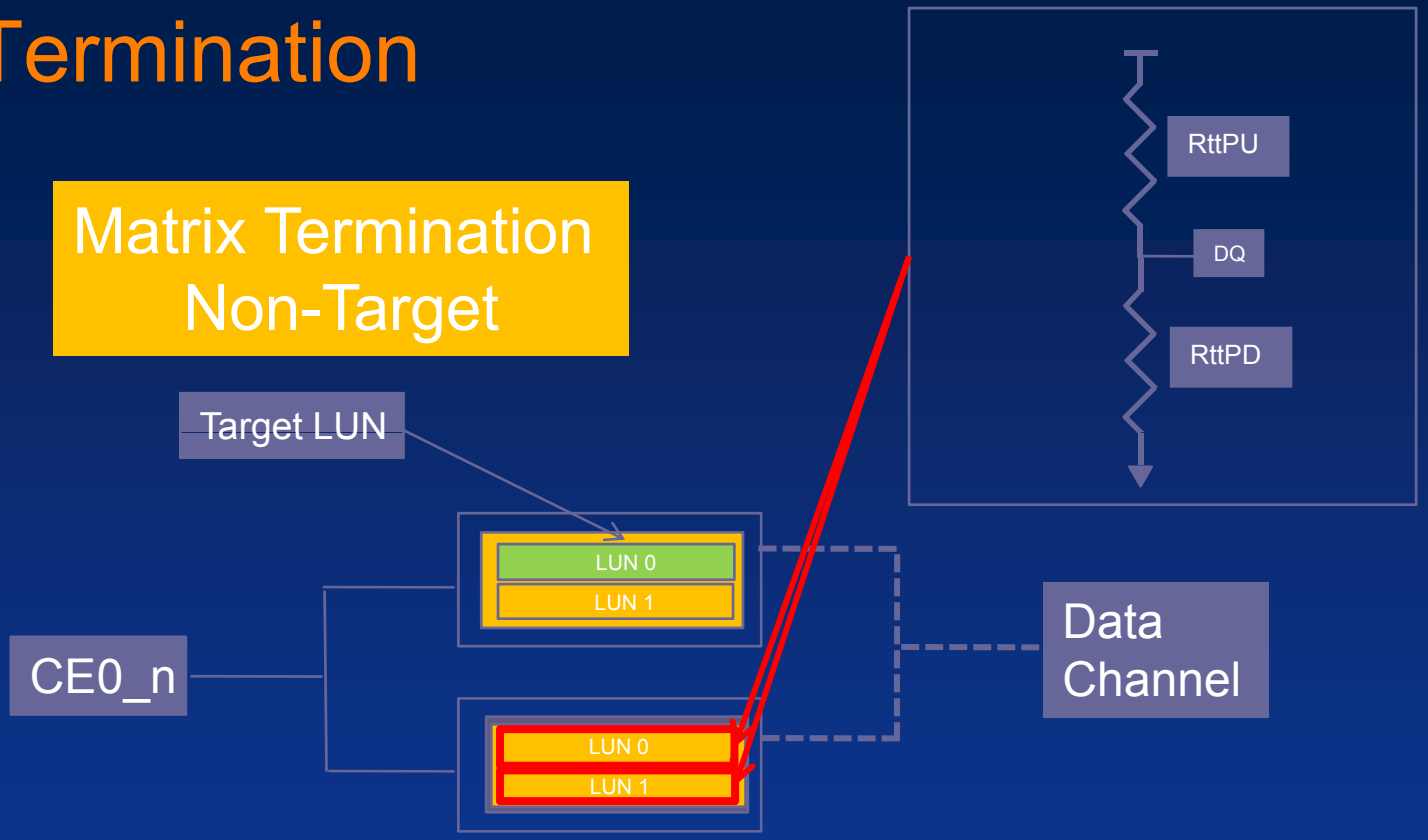
- Target only termination available
- If supported for reads, output drivers cannot be used for termination

Matrix Termination vs. Self Termination



- Target or non-target termination capable
- Supported for reads and writes

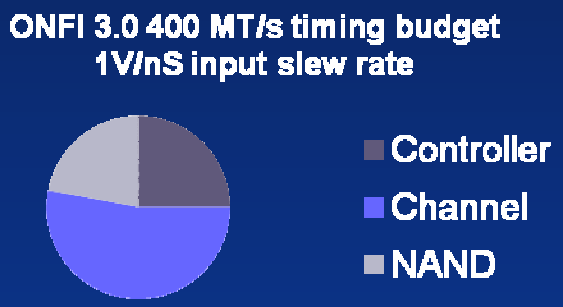
Matrix Termination vs. Self Termination

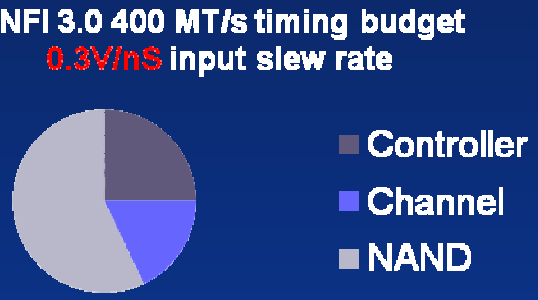


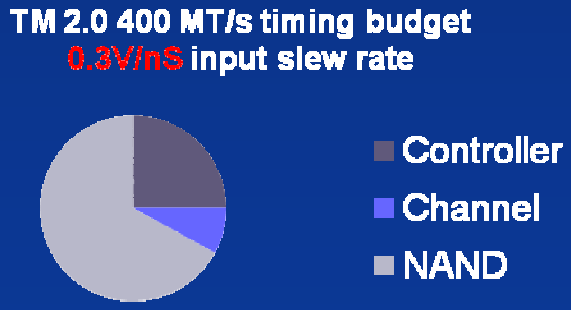
- Multiple LUNs can be terminators, providing a flexible array of termination values and locations

Timing Budget Considerations

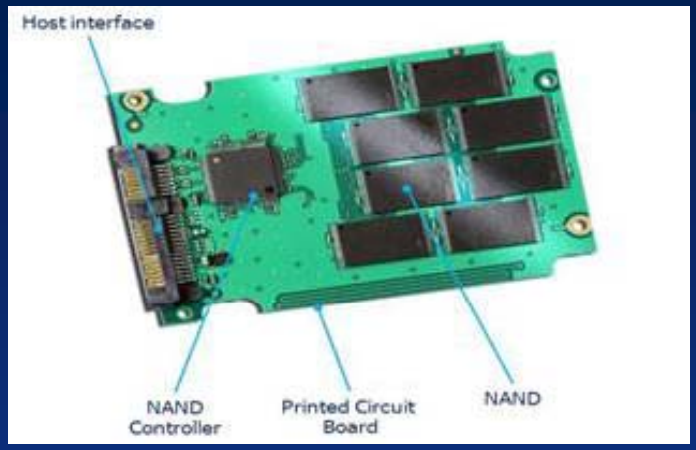
- With heavy loading and long trace lengths, slew rates can become very slow.

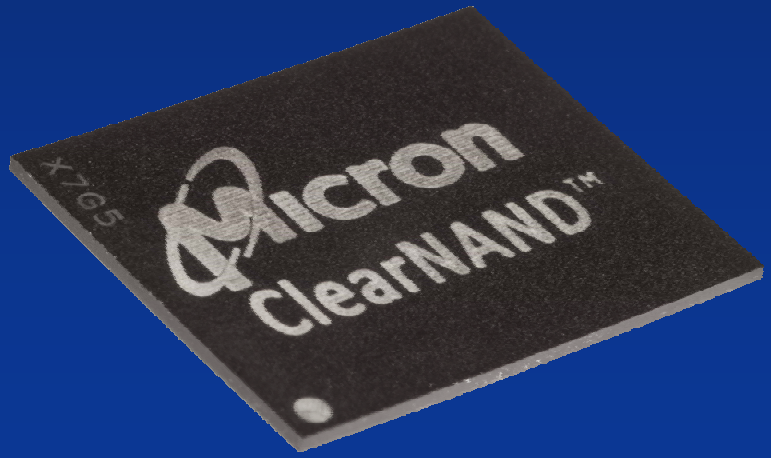






Topology Considerations





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