

Overcoming (or Embracing) the Dreaded Single-Source Dilemma

Michael Abraham (mabraham@micron.com)
Applications Engineering Manager
Micron Technology, Inc.



Agenda

- An introduction to NAND Flash
- How to multisource
- Why single source?
- Alternatives to single sourcing

An Introduction to NAND Flash

- NAND Flash is made for data storage
 - High density: 128MB–16GB per package
 - Low cost per bit
 - Low power
 - Nonvolatile

NAND Structure

- NAND array is page- and block-centric
 - Page is the smallest programmable and readable unit in the NAND array composed of bytes or words
 - Block is the smallest erasable unit composed of many pages

- NAND interface
 - Sequential data input and output preferred
 - Commands, addresses, and data I/O share 8 or 16 I/Os (multiplexed bus)

Lots of Density Growth

- NAND Flash is perfect for density scaling
 - Cell layout perfect for process shrinks
 - Fixed pin count leads to consistent packaging options
 - Multiple die stack within a package
 - Multi-level cell (MLC) stores more bits of data per cell

- Result each year
 - Twice the density
 - Roughly the same die size

Market Segments

- Entering many market segments
 - Automotive: Car stereo and navigation
 - Computing: SSD, HDD, and caching
 - Consumer: Cards, DSC, GPS, MP3, and video
 - Wireless: Mobile phones
 - More...

Many NAND Suppliers

- Suppliers include
 - Hynix
 - Intel
 - Micron
 - Samsung
 - STMicroelectronics
 - Toshiba

- With many suppliers, NAND is easy to second source, right?

NAND Configuration Options

- **Vcc**
 - 3.3V
 - 1.8V
- **I/O width**
 - x8
 - x16
- **Page size**
 - 2,112 bytes
 - 4,224 bytes
 - 4,314 bytes
 - More coming...
- **Number of planes**
 - 1
 - 2
- **Density**
 - 1–128Gb per package
- **ECC**
 - 1 bit
 - 4 bits
 - 8+ bits
- **Number of partial page programs (NOP)**
 - SLC: 4, 8
 - MLC: 1
- **Endurance**
 - SLC: 100,000 cycles
 - MLC: $\leq 10,000$ cycles
- **Temperature range**
 - Commercial (0°C to +70°C)
 - Wireless (–25°C to +85°C)
 - Extended (–40°C to +85°C)
- **Package**
 - TSOP
 - BGA
 - LGA
 - MCP

Most Common Configurations

- For 3.3V: x8 SLC/MLC, commercial temp, TSOP
 - Most widely available configuration
 - SLC for performance and endurance
 - MLC for density and lowest cost per bit

- For 1.8V: x16 SLC, commercial temp, BGA/MCP
 - Common for wireless/embedded applications
 - Typically SLC only, but not as high of performance as 3.3V x8 SLC
 - 100,000 cycles with 1-bit ECC is usually important
 - Typically in BGA or MCP since board real estate is important

The Multisource Dilemma

- Even when picking a common configuration, differences exist in NAND Flash parts
 - Protocol
 - Array addressing
 - Features
 - ECC requirements
 - Page size
 - More...

- Having a multisource is not impossible, it just requires more upfront work

Step #1: Pick the Right NAND Controller

- Does it have enough ECC for the future?
 - For SLC: Recommend 4-bit RS or BCH
 - For MLC: Recommend 8+ bits BCH

- Can it support NOP = 1?
 - For SLC: Improves endurance
 - For MLC: Already required

- Does it support x8 and/or x16?

- Does it support single- and multi-plane operations?

Step #1: Pick the Right NAND Controller (continued)

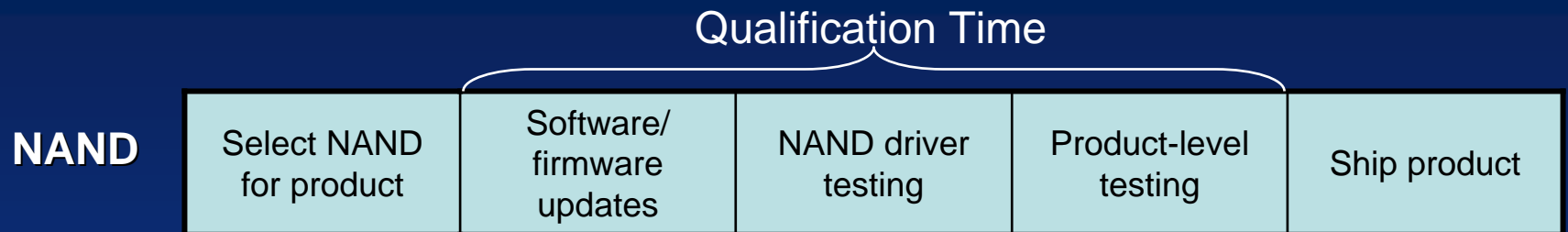
- Does it need to support MLC NAND?
 - Typically, once MLC is supported, SLC is also supported
- Does it have a good firmware/software SDK?
 - Command protocol
 - Advanced features (cache operations, unique ID, etc.)
 - Addressing
 - Page size
 - Block management/wear leveling
 - SLC/MLC support
- Does it support EDO timing if needed?
 - Determines which edge the controller latches data from the NAND
- Does it support “Boot from NAND” if this feature is needed?

Step #2: Select the NAND Flash

- Plan upfront to support multiple vendors
- Determine whether your application can support MLC NAND Flash
- Compare data sheets to look for differences in:
 - Op codes and command sequences
 - Page size
 - 2,000 or 4,000?
 - How many spare area bytes? 16 per each 512 bytes of data? More?
 - Array addressing: Where are the plane-select bits?
 - Toshiba: High-order address bits under the die-select bits
 - Others: Low-order address bits just above the page address
 - Multi-plane address formats
 - Samsung: Ignore the first address; look only at the die- and plane-select bit since adjacent blocks in planes are paired
 - ONFI: Full address must be specified for first address since adjacent blocks in planes may not be paired
 - Timing parameters
 - How fast can I transfer data over the I/Os?
 - Does the part support EDO?
 - ECC



Typical Development Cycle for NAND-Based Products



- NAND development process can be time consuming
- Each new device, even from the same vendor, requires some kind of firmware/software support
- Typically requires look-up table for each part based on Read ID to identify each device

How Does ONFI Fit In?

- ONFI provides consistency across participating NAND vendors
 - Command set
 - Protocol
 - Array addressing
 - Package definition
 - Timing parameters
 - Defect mapping



OPEN NAND
FLASH INTERFACE

Parameter Page Describes Device Capabilities to the Controller

- Once ONFI is supported in the controller, it reduces qualification time for new ONFI parts

ONFI NAND

Supplier samples new NAND	Product-level testing	Ship product
---------------------------	-----------------------	--------------

- Firmware may need to be modified for optional features if not already supported
- The controller is able to query the NAND for its capabilities by reading the parameter page
 - Array architecture (single- or multi-plane, page size, etc.)
 - Minimum ECC requirements
 - Timing parameters supported
 - More...

The NAND Trade-Off

- Long development times
 - Can be shortened by ONFI support, but not all vendors support ONFI
- The controller is required to provide
 - ECC
 - Block management
 - Wear leveling
- Result: Lowest cost-per-bit memory
 - Saves the most money, particularly for high-volume products

Why Single Source?

- Time to market is critical
- Small budget for development
- Low volume
- A “must have” feature not found commonly on other NAND devices
 - High-performance throughput requirement
 - Needed density is not yet widely available
 - OTP
 - Block lock

Why Is Single Sourcing Risky?

- May inadvertently lock into niche feature(s), making future firmware/software updates more difficult
 - OTP
 - Block lock
 - PRE
- Component price goes up
- Part allocation
- EOL

Alternatives to Single Sourcing

- Use software/firmware vendor for file system, flash translation layer, and/or low-level driver support
 - Performs block management and wear leveling
 - Supports multiple NAND vendors
 - Works with variety of controllers
 - Supports variety of operating systems

- Select an embedded memory that uses NAND technology
 - eMMC – MultiMediaCard interface
 - SD – Secure Digital interface
 - DOC – NOR-like interface
 - OneNAND – NOR-like interface
 - LBA NAND – NAND interface
 - BA NAND – NAND interface

Embedded Memories

■ Pros

- Most handle ECC, block management, and wear leveling
- eMMC, SD, OneNAND, and DOC have multiple vendor sources
- eMMC, SD, and BA NAND follow industry-standard interfaces allowing for compatibility across vendors
- Requires less development cost up front

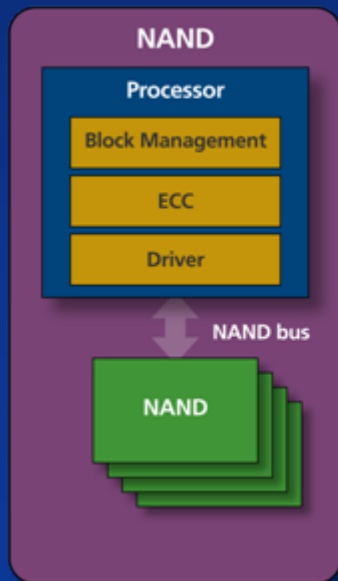
■ Cons

- Cost more per bit than NAND
- May require new controller to support the particular interface
- Some solutions are vendor proprietary like OneNAND and LBA NAND
- Highest densities will lag NAND densities

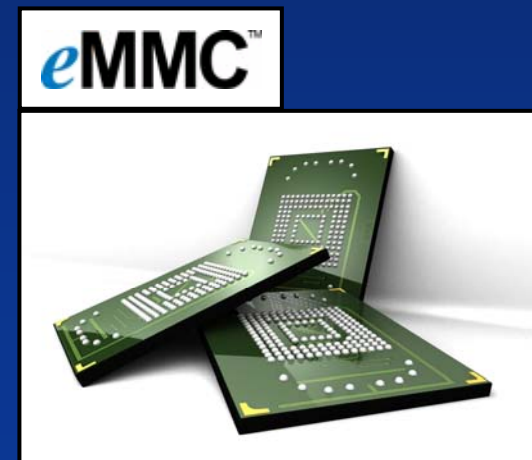
eMMC Example

- Interface and packaging standardized by MMCA and JEDEC
- MMC interface found already on many wireless controllers today
- eMMC vendors
 - Micron (Managed NAND)
 - Samsung (MoviNAND)
 - Toshiba (eMMC NAND)

Direct NAND Interface



Managed NAND



Conclusion

- NAND Flash market is growing significantly for storage
- With upfront planning and some development cost, it is possible to multisource NAND Flash and keep volume price down
- ONFI simplifies the multisourcing by reducing design and qualification effort for additional NAND products
- There are some reasons to single source, but some risks too
- Other NAND-based memories can simplify design and qualification effort

References

- Memory vendors
 - Hynix: <http://www.hynix.com/>
 - Intel: <http://www.intel.com/>
 - Micron:
<http://www.micron.com/nand/>
 - Samsung: <http://www.samsung.com/>
 - SanDisk: <http://www.sandisk.com/>
 - ST: <http://www.st.com/>
 - Toshiba:
<http://www.toshiba.com/taec/>

- Interface standards organizations
 - ONFI: <http://www.onfi.org/>
 - SD: <http://www.sdcard.org/>
 - MMCA: <http://www.mmca.org/>
 - JEDEC: <http://www.jedec.org/>

- Flash file system vendors
 - CMX Systems: <http://www.cmx.com/>
 - Datalight: <http://www.datalight.com/>

About Michael Abraham

- Manager of Micron's NAND Flash Applications Engineering group
- BS in Computer Engineering from Brigham Young University
- Micron's representative on the ONFI technical committee
- Key role in defining and standardizing the new high-speed NAND interface within Micron and at ONFI

