



## ONFI Standards and What They Mean to Designers

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# NAND Flash Inconsistencies Without ONFI

- Device identification using read ID
- Array architecture and addressing
- Command set
- Timing parameters
- ECC and endurance
- Factory-marked bad blocks
- Device behavior and status

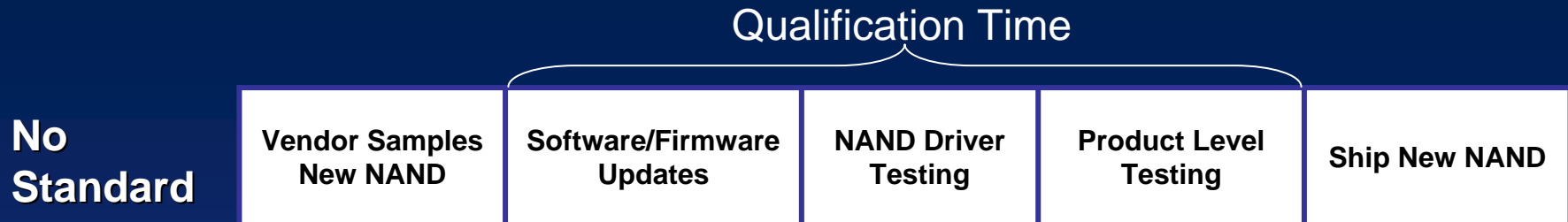
# Answering Questions

NAND Flash devices must answer basic questions to simplify software development and support:

- What is the page size (data and spare)?
- How many pages per block?
- How many blocks per die?
- How many die per CE#?
- Is the device multi-plane?
- How do I address the device?
- What advanced commands are supported?
- What timing parameters does this device support for normal and cache operations?
- How many bits of ECC are required?
- What is the block endurance?

These are *not* answered by read ID, especially across multiple NAND vendors.

# End Result Without ONFI



- What are the effects of not having NAND standardization?
  - Long firmware/software development cycles and updates
  - Long test/verification cycles
  - Firmware/software changes for *each* new NAND Flash device
  - Products are slow to market
  - NAND Flash evolving faster than product lifecycles, which makes product continuity difficult if firmware/software must be rewritten to support new NAND devices

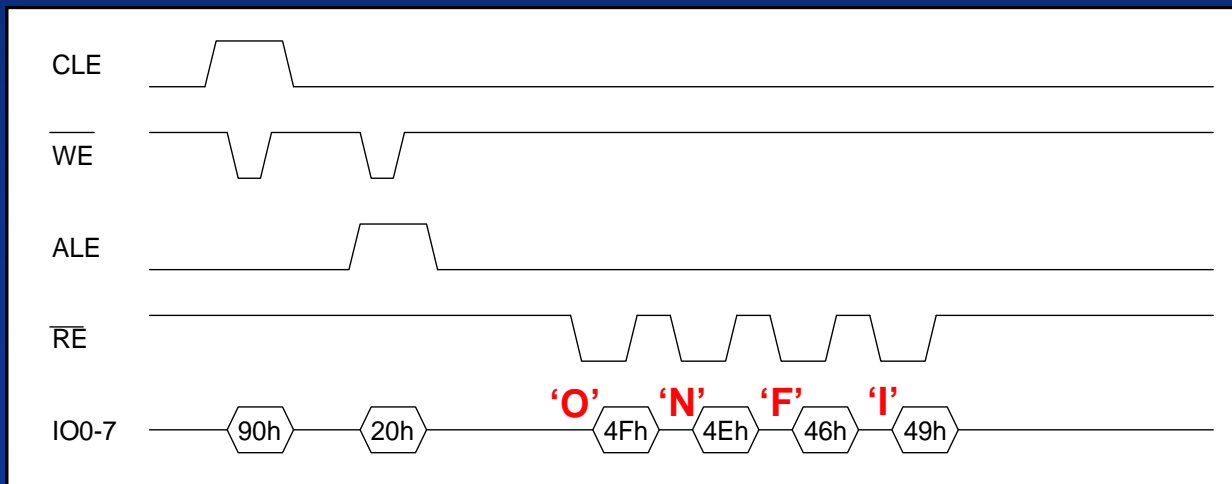
# NAND Identification with ONFI

- Read ID and the parameter page
  - Device identification
  - Array architecture and addressing
  - ECC and block endurance
  - Timing modes
- Command set
- Bad block handling



# Read ID

- Read ID used today to identify each NAND device
- Using an address of 20h returns the ONFI signature and indicates that the polled device includes a parameter page



# Parameter Page

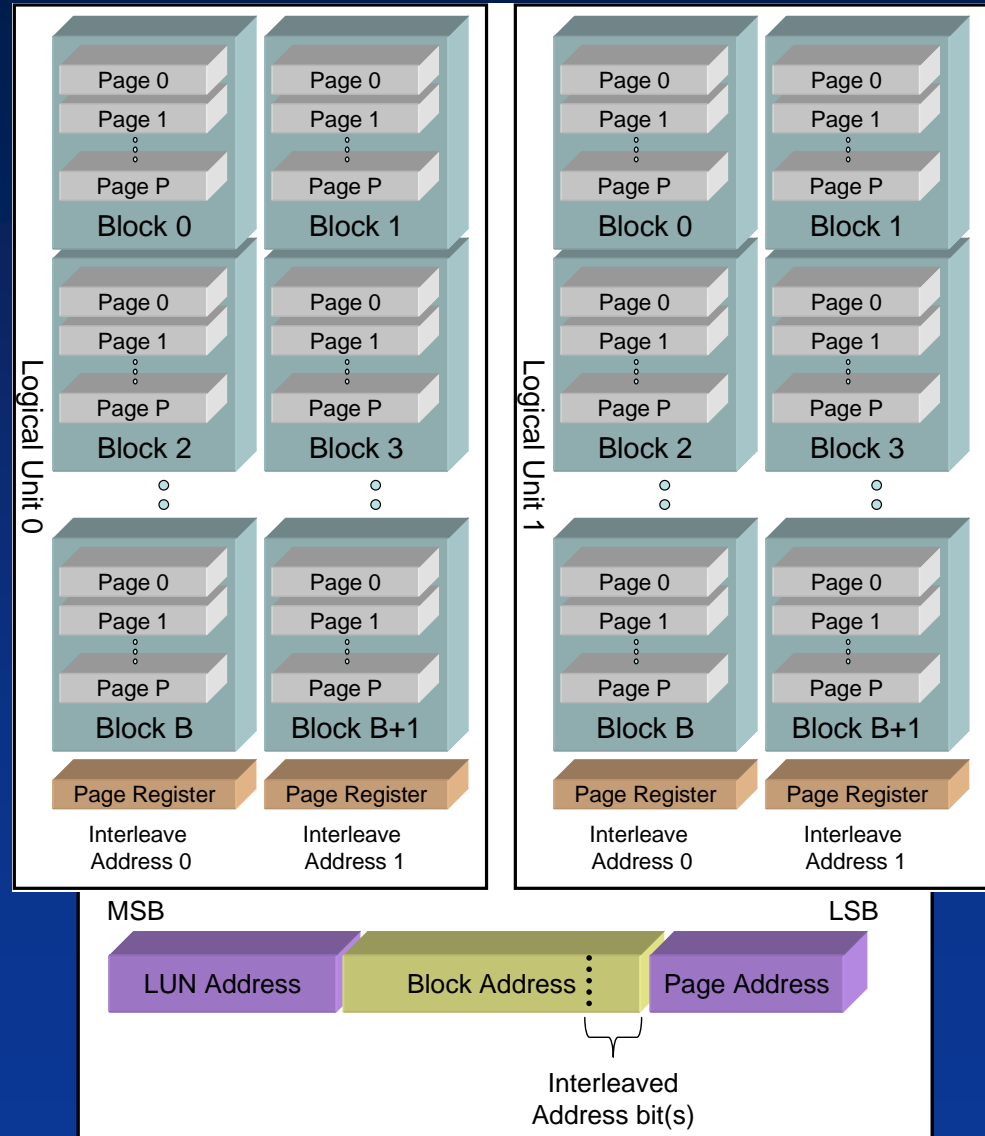
- Parameter page describes the device's capabilities
- Sections within the parameter page
  - Revision information
  - Features
  - Manufacturer information
  - Memory organization
  - Device timing
  - Vendor-specific area

## Memory Organization Block of Parameter Page

- Number of data bytes per page
- Number of spare bytes per page
- Number of pages per block
- Number of blocks per logical unit (LUN)
- Number of logical units
- Number of address cycles
- Number of bits per cell
- Block endurance
- Number of programs per page
- Number of bits of ECC correction
- Interleaved addressing

# Architecture and Addressing

- ONFI uses abstraction because it defines behavior, not an implementation method
- The following ONFI terms are mapped to terms commonly used in NAND implementation:
  - Target: CE#
    - A packaged NAND device has one or more targets
    - A target is completely independent of other targets
  - Logical unit (LUN): die
    - A target has one or more LUNs
    - Each LUN is operationally independent of other LUNs on the same target
    - LUN address bits are above the block address bits
  - Interleaved address: plane
    - All interleaved operations must be the same type (program or erase)
    - Interleaved address bit(s) are the lowest order block address bits
    - Adding interleaved read to ONFI 2.1



# Command Set

- Provides consistent, defined commands
- Advanced commands are optional (“O”)
- The parameter page indicates whether optional commands are supported by the device
- Target level commands are indicated for the behavioral flow

Command	O/M	1 <sup>st</sup> Cycle	2 <sup>nd</sup> Cycle	Target level commands
Read	M	00h	30h	
Copyback Read	O	00h	35h	
Change Read Column	M	05h	E0h	
Read Cache Enhanced	O	00h	31h	
Read Cache	O	31h		
Read Cache End	O	3Fh		
Block Erase	M	60h	D0h	
Interleaved	O		D1h	
Read Status	M	70h		
Read Status Enhanced	O	78h		
Page Program	M	80h	10h	
Interleaved	O		11h	
Page Cache Program	O	80h	15h	
Copyback Program	O	85h	10h	
Interleaved	O	85h	11h	
Change Write Column	M	85h		
Read ID	M	90h		Y
Read Parameter Page	M	ECh		Y
Read Unique ID	O	EDh		Y
Get Features	O	EEh		Y
Set Features	O	EFh		Y
Reset	M	FFh		Y

## Read Cache Enhanced (00-31h)

- Permits reading random pages anywhere on a LUN; important for computing applications
- Better performance than multi-plane page read since hidden  $t_R < IO$  time
- No page address restrictions, unlike multi-plane page read, which requires page address to be the same
- Command sequence:
  - Issue 00h-5A-30h (op A); wait for  $t_R$
  - Issue 00h-5A-31h (op B); wait  $t_{RCBSY}$
  - Read data from op A
  - Issue 3Fh; wait  $t_{RCBSY}$
  - Read data from op B

## Read Status Enhanced (78h)

- Reads status on any LUN
- LUN status register bits
  - Bits 6 and 5 are generic
  - Bits 1 and 0 are specific to the selected interleaved address
- Changes data output between LUNs
  - Issue 00h command following read status enhanced for data output
  - Ignores interleaved address bits and only selects the LUN
  - Previously selected interleaved address outputs data
- Single command reduces burden of requiring a separate status command for each LUN (such as F1h, F2h, and so on)

## Get Features (EEh), Set Features (EFh)

- Was not highly used in the ONFI 1.0 specification
- Used in ONFI 2.0 to cover setting of:
  - Output drive impedance
  - Interface type (legacy or DDR)
  - Interface timing mode
- Includes vendor-specific feature address space to handle the following:
  - OTP
  - R/B# pull-down strength
  - More...
- Reduces the need to add more vendor-specific instructions to the command set

# Timing Parameters

- Timing modes represent the timing parameters

Mode	$t_{RC}$	$t_{WC}$	Unit
0	100	100	ns
1	50	45	ns
2	35	35	ns
3	30	30	ns
4	25	25	ns
5	20	20	ns

- Supported timing modes are specified in the parameter page
- Provides consistent timing for controllers
- Controllers can operate slower than the published timing mode if not capable of fastest operation

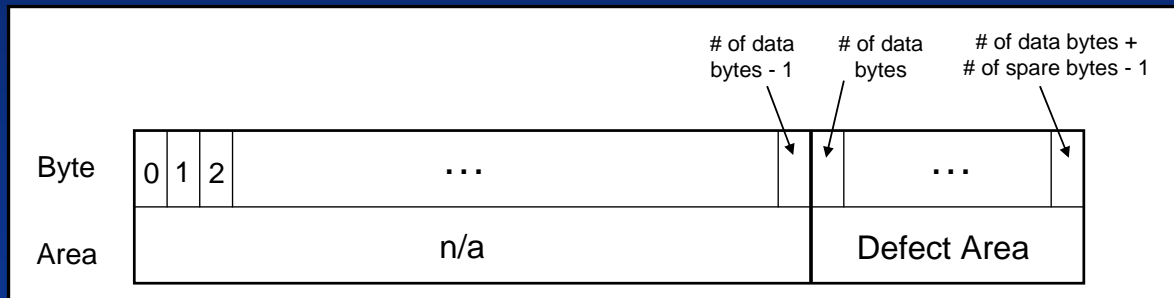
# An Example: Timing Mode 4

- Each parameter clearly specified
- All parameters' edges described in text, and most are drawn in figures

Parameter	Mode 4		Unit	Parameter	Mode 4		Unit
	Min	Max			Min	Max	
<sup>t</sup> ADL	70	—	ns	<sup>t</sup> RC	25	—	ns
<sup>t</sup> ALH	5	—	ns	<sup>t</sup> REA	—	20	ns
<sup>t</sup> ALS	10	—	ns	<sup>t</sup> REH	10	—	ns
<sup>t</sup> AR	10	—	ns	<sup>t</sup> RHOH	15	—	ns
<sup>t</sup> CEA	—	25	ns	<sup>t</sup> RHW	100	—	ns
<sup>t</sup> CH	5	—	ns	<sup>t</sup> RHZ	—	100	ns
<sup>t</sup> CHZ	—	30	ns	<sup>t</sup> RLOH	5	—	ns
<sup>t</sup> CLH	5	—	ns	<sup>t</sup> RP	12	—	ns
<sup>t</sup> CLR	10	—	ns	<sup>t</sup> RR	20	—	ns
<sup>t</sup> CLS	10	—	ns	<sup>t</sup> RST	—	5/10/500	μs
<sup>t</sup> COH	15	—	ns	<sup>t</sup> WB	—	100	ns
<sup>t</sup> CS	20	—	ns	<sup>t</sup> WC	25	—	ns
<sup>t</sup> DH	5	—	ns	<sup>t</sup> WH	10	—	ns
<sup>t</sup> DS	10	—	ns	<sup>t</sup> WHR	60	—	ns
<sup>t</sup> FEAT	—	1	μs	<sup>t</sup> WP	12	—	ns
<sup>t</sup> IR	0	—	ns	<sup>t</sup> WW	100	—	ns

# Factory-Marked Bad Blocks

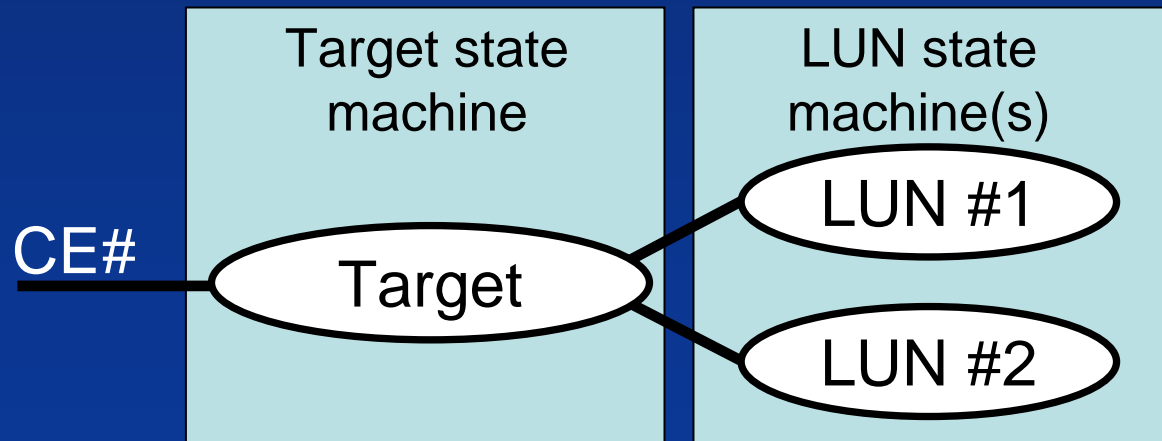
- Factory-marked bad blocks are now standardized for SLC *and* MLC, so both use the same algorithm
- The block is factory-marked bad if the first byte is 00h (or the first word is 0000h) in the “defect area” in the first or last page of the block
- Defect area



- MLC devices ship today without blocks being “pristine”; some defects may exist in good blocks

# Device Behavior and Status

- Behavioral flow shows how the device operates
  - Target state machine
    - Handles read ID, read parameter page, and unique ID
    - Passes LUN operations to the correct LUN (based on address)
  - LUN state machine
    - One LUN state machine per LUN in the target
    - Handles anything that can be done in a multi-LUN operation, such as read page, program page, erase block
  - Provides consistent command and status behavior among vendors, greatly simplifying firmware for controllers



# What are ONFI Shortcomings?

- No interleaved (multi-plane) read page
  - Coming in ONFI 2.1
  
- Not accepted by all NAND vendors
  - Would you rather write firmware for eight different NAND vendors or for the equivalent of three?
  - Micron extends open invitation to the last two NAND vendors to join ONFI
  
- ONFI describes device capabilities, but it doesn't eliminate nonsoftware-related issues
  - ONFI describes ECC requirements, but it can't make up for a lack of ECC support on the host controller
  - ONFI BA NAND (specification now available) provides a simpler NAND interface, including block management and ECC

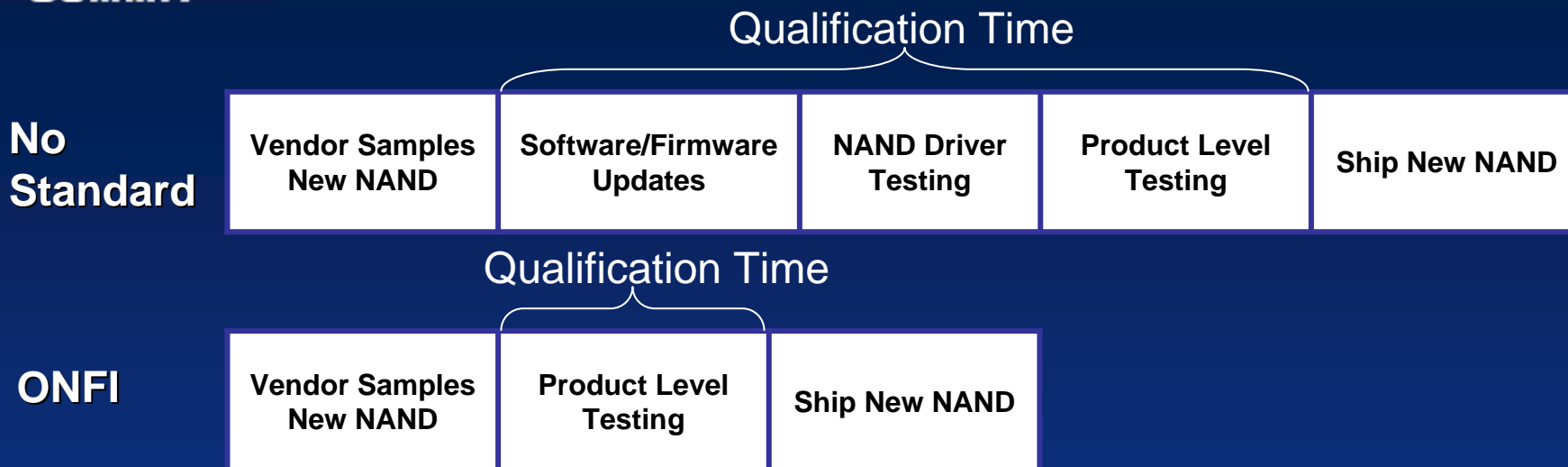
# NAND Flash Consistencies After ONFI

- Device identification using the parameter page
- Array architecture and addressing
- Command set
- Timing modes and parameters
- ECC and endurance
- Factory-marked bad blocks
- Device behavior and status

# Other Concepts in the ONFI Specification

- Packaging pinout/ballouts
  - 48-pin Type-I TSOP
  - 63-ball BGA
  - 52-pad LGA with dual x8 interface
  - 100-ball BGA with dual x8 interface
  
- Electrical interface
  
- Power-on behavior
  
- Discovery and initialization
  
- Pin capacitance

# End Result with ONFI



- What are the effects of ONFI standardization?
  - Ability to write flexible firmware up front that supports various NAND architectures, page sizes, and vendors
  - Ability to shorten or eliminate the need for firmware/software updates for *each* new NAND device
  - Faster time to market

## For More Information on ONFI

- ONFI specifications are publicly downloadable at <http://www.onfi.org/>
- ONFI membership is available to all; currently 85+ companies participate
- There are currently no membership dues



## About Michael Abraham

- Manager of Micron's NAND Flash Applications Engineering group
- B.S. in Computer Engineering from Brigham Young University
- Micron's technical representative in ONFI and JEDEC for NAND Flash
- Key role in defining and standardizing the new high-speed NAND interface within Micron and at ONFI



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